0.8μm CMOS-Mixed Mode Designer's Handbook (Version 1.4)

2005. 05. 05

Semiconductor Process

Research Department

Electronics and Telecommunications

Research Institute

Contents

1. Scope

This Document contains information related to dimensions of the limiting topological design rule and provides users with electrical design limits for 0.8㎛ Analog CMOS processes.

This process contains poly Ⅰ/Ⅱ capacitors and poly Ⅱ resistors.

All of the measurements are done at room temperatures. The typical values are inferred from measured data, while the maximum and the minimum values have been estimated from the process limits.

2. Design Rule

2.1 Layout Information

2.1.1 The dimensions are expressed in units of lambda and micron. The conversion between lambda and micron is defined as :

Micron = Lambda x 0.4

2.1.2 Description of drown layers :

NWL	N-Well
ACT	N+ & P+ Actives
PL1	Poly Ⅰ
PL2	Poly Ⅱ
NSD	N+ Implant
PSD	P+ Implant
CNT	Contact
ME1	Metal Ⅰ
VIA	Via
ME2	Metal Ⅱ
PAD	Pad

2.2 Drawing Rules

2.2.1 Table of Layer Symbols

Symbol	Layer	Description	Pattern
NWL	N-Well	Defines substrate of p-channel devices	
ACT	N+ & P+ Actives	Defines n+/p+ diffused and p/n-channel gate area	N P
PL1	Poly Ⅰ	Defines poly gates and poly interconnects	
PL2	Poly Ⅱ	Defines poly resistors and poly capacitors	
NSD	N+ Implant	Defines n+ ion implant areas	
PSD	P+ Implant	Defines p+ ion implant areas	
CNT	Contact	Defines contact openings to diffusion and poly Ⅰ, Ⅱ	
ME1	Metal Ⅰ	Defines first metal interconnects	
VIA	Via	Defines openings in the insulator between metal Ⅰ and Metal Ⅱ	
ME2	Metal Ⅱ	Defines second metal interconnects	
PAD	Pad	Defines opening in the passivation layer for bonding	

2.2.2 General Description of the Rules

Rules	Lambda(0.4μm)	μm	Rule #	Field
Grid :				
Size	0.25	0.1		
NWL :				DARK
Pitch	15.0	6.0		
Width	10.0	4.0	NW1	
Width(Resistor)	25.0	10.0	NW2	
Space(same potential)	5.0	2.0	NW3	
Space(diff. potential)	20.0	8.0	NW4	
ACT(Align to NWL) :				CLEAR
Pitch	6.0	2.4		
Pitch@Contact	8.5	3.4		
Width(interconnection)	2.5	1.0	AC1	
Width(TR)	3.5	1.4	AC2	
Space	2.5	1.0	AC3	
P+ in NW to N+ in PW Space	12	4.8	AC4	
NW OL of P+	6.0	2.4	AC5	
NW OL* of N+	3.0	1.2	AC6	
NW space to N+	6.0	2.4	AC7	
NW space to P+	3.0	1.2	AC8	
N+ GR** OL of NW	6.0	2.4	AC9	
P+ GR OL of PW	6.0	2.4	AC10	

* : overlap

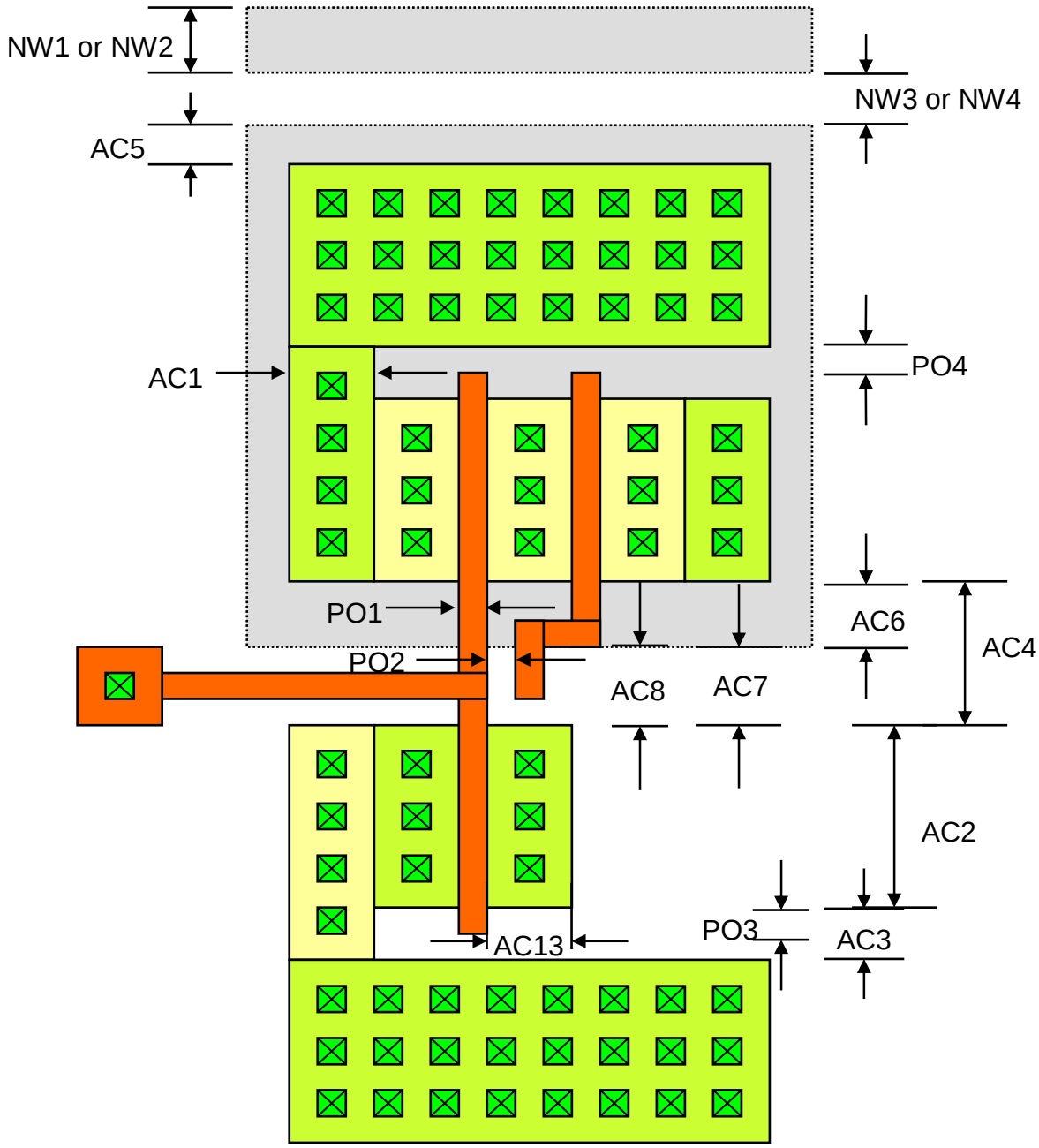
** : guard ring

Rules	Lambda(0.4μm)	μm	Rule #	Field
N+ GR space to P+ in PW	4.0	1.6	AC11	
N+ GR space to P+ in PW	4.0	1.6	AC12	
Extension over gate	3.5	1.4	AC13	
FVT(Align to ACT)				CLEAR
same as NWL				
PL1(Align to ACT)				CLEAR
Pitch	4.5	1.8		
Pitch@Contact	8.0	3.2		
Width	2.0	0.8	PO1	
Space	2.5	1.0	PO2	
End Cap	2.5	1.0	PO3	
Space to Act	1.25	0.5	PO4	
PL2(Align to ACT)				CLEAR
as resistor				
Pitch	4.5	1.8		
Pitch@Contact	8.0	3.2		
Width	2.0	0.8	PL1	
Space	2.5	1.0	PL2	
Space to Poly Ⅰ	2.5	1.0	PL3	
Space to Act	2.0	0.8	PL4	

Rules	Lambda(0.4μm)	μm	Rule #	Field
as capacitor				
1) in case of Poly II is smaller than Poly I				
Poly I OL of Poly II	1.0	0.4	PL5	
Space to Act	2.0	0.8	PL6	
2) in case of Poly II is larger than Poly I				
Poly II OL of Poly I	1.0	0.4	PL7	
Space to Act	2.0	0.8	PL8	
NSD(Align to ACT) :				DARK
Width	5.0	2.0	NI1	
Space to P+ Act	1.25	0.5	NI2	
OL of Poly I or Poly II	1.25	0.5	NI3	
OL of Act	1.25	0.5	NI4	
PSD(Align to ACT) :				DARK
Width	5.0	2.0	PI1	
Space to P+ Act	1.25	0.5	PI2	
OL of Poly I or Poly II	1.25	0.5	PI3	
OL of Act	1.25	0.5	PI4	
CNT(Align to ACT) :				DARK
Pitch	4.0	1.6		
Size	2.0	0.8	CO1	
Space	2.0	0.8	CO2	
Act OL	2.0	0.8	CO3	

Rules	Lambda(0.4μm)	μm	Rule #	Field
Poly Ⅰ, Ⅱ OL	2.0	0.8	CO4	
ME1 OL	2.0	0.8	CO5	
Space to Poly Ⅰ, Ⅱ	2.0	0.8	CO6	
Poly Ⅰ Contact to Act space	3.0	1.2	CO7	
Poly Ⅰ Contact to Poly Ⅱ				
Poly Ⅱ capacitor	2.0	0.8	CO8	
Poly Ⅱ resistor	4.5	1.8	CO9	
Overlapping Poly Ⅰ/Ⅱ structure	2.0	0.8	CO10	
Poly Ⅱ Contact to Poly Ⅰ				
Poly Ⅰ unrelated	4.5	1.8	CO11	
Overlapping Poly Ⅰ/Ⅱ structure	2.0	0.8	CO12	
ME1(Align to ACT) :				CLEAR
Width	3.0	1.2	M11	
Space	2.0	1.2	M12	
Space(width ≥ 6 lambda)	4.0	1.6	M13	
Space(width ≥ 25 lambda)	5.0	2.0	M14	
VIA(Align to ME1)				DARK
Size	2.0	0.8	VI1	
Space	2.0	0.8	VI2	
ME1 OL	2.0	0.8	VI3	
ME2 OL	2.0	0.8	VI4	
Space to Contact	2.0	0.8	VI5	
Space to Poly Contact	2.0	0.8	VI6	

Rules	Lambda(0.4μm)	μm	Rule #	Field
ME2(Align to ME1) :				CLEAR
Width	3.0	1.2	M21	
Space	2.0	1.2	M22	
Space(width ≥ 6 lambda)	4.0	1.6	M23	
Space(width ≥ 25 lambda)	5.0	2.0	M24	
PAD(Align to ME1) :				DARK
Size	250	100		
Space	200	80		
ME1 OL	25	10.0		
Via OL	12	5.0		
Me2 OL	25	10.0		
Space to Active	50	20.0		


NW1 or NW2
NW3 or NW4
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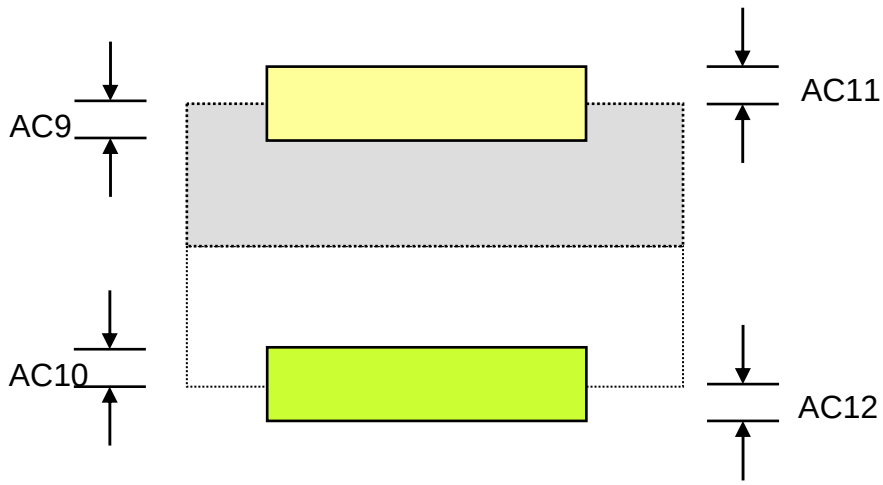
AC1
PO4
PO1
PO2
AC6
AC4
AC8
AC7
AC2
PO3
AC3
AC13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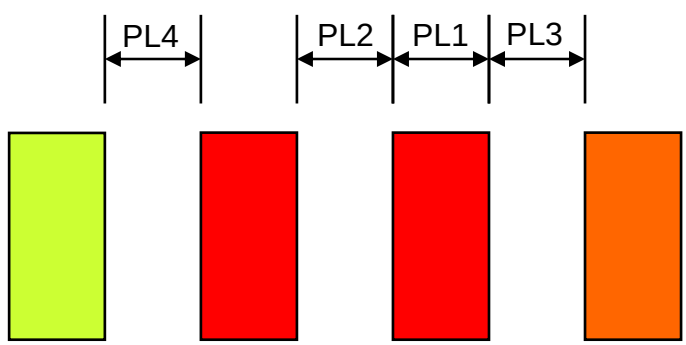
AC10
AC12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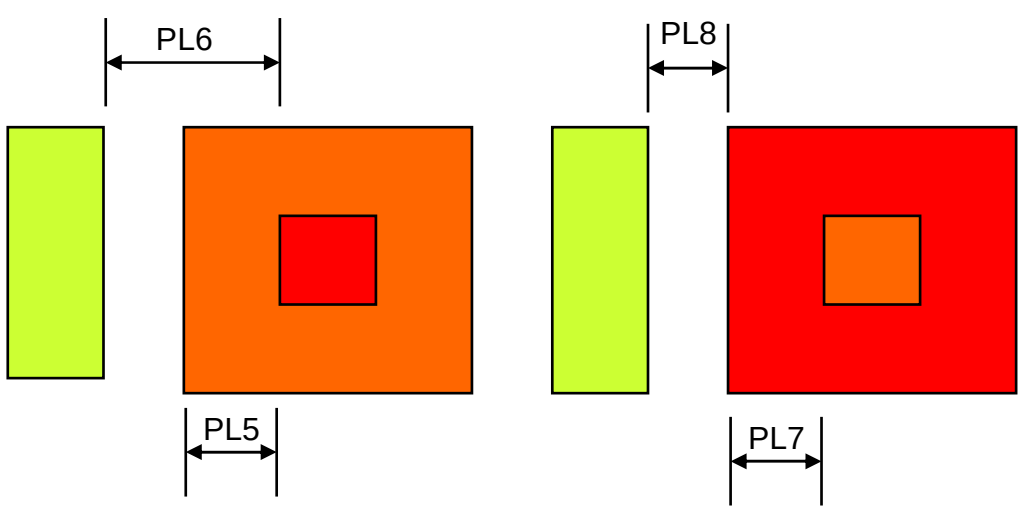
PL1
PL3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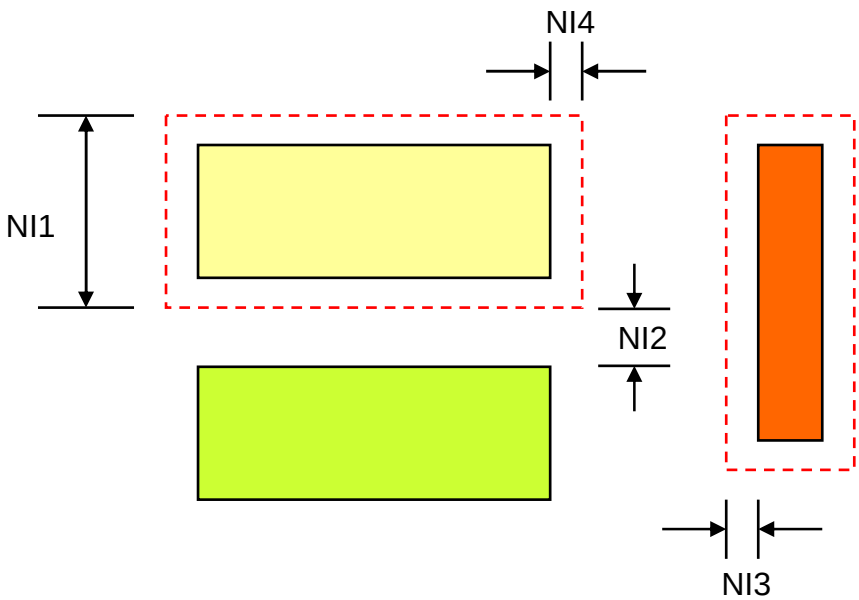
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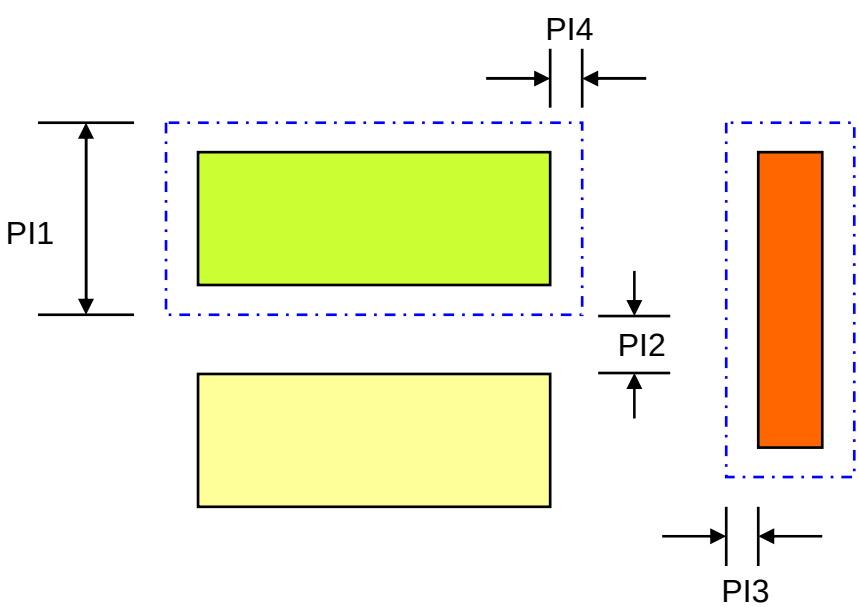
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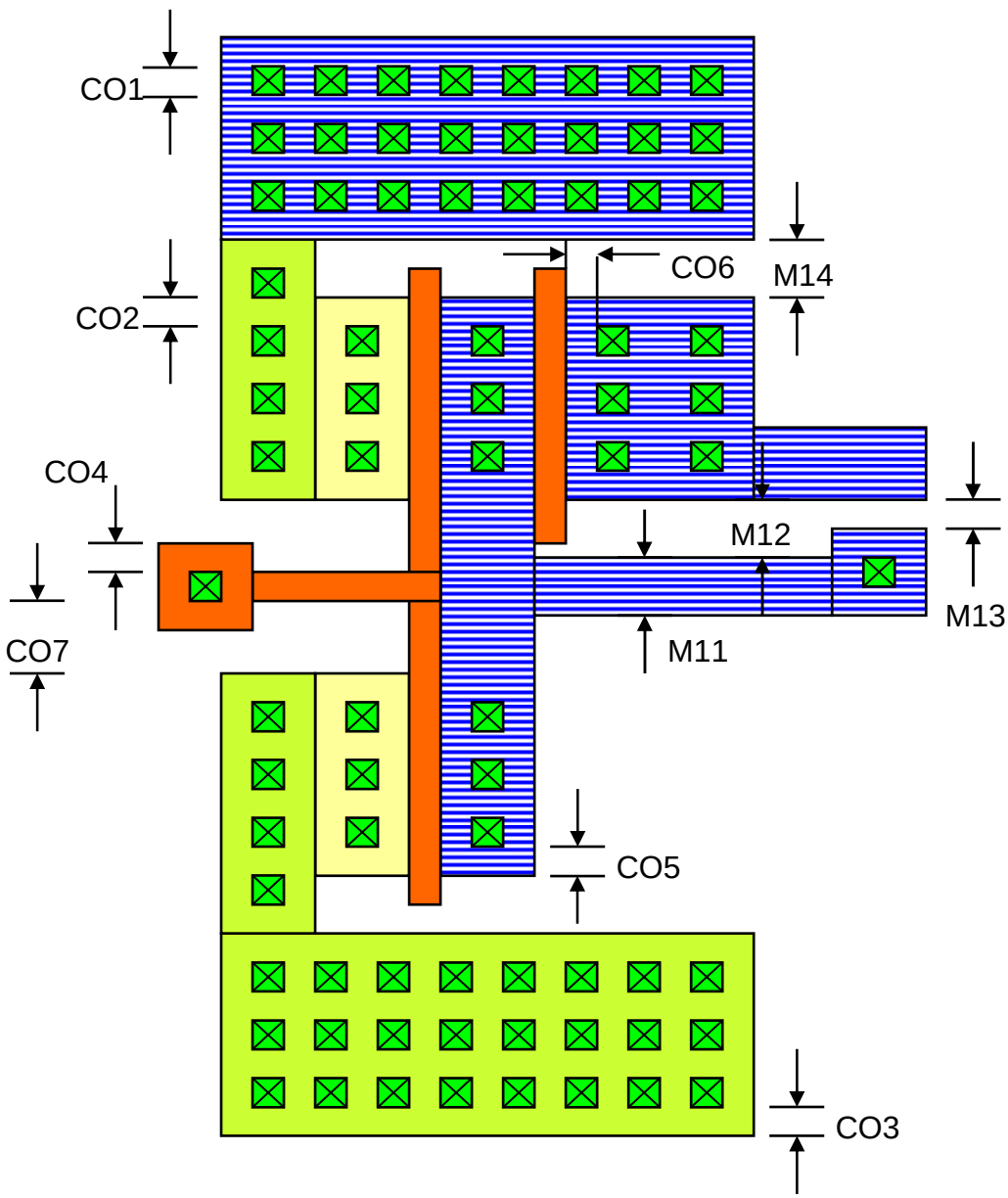
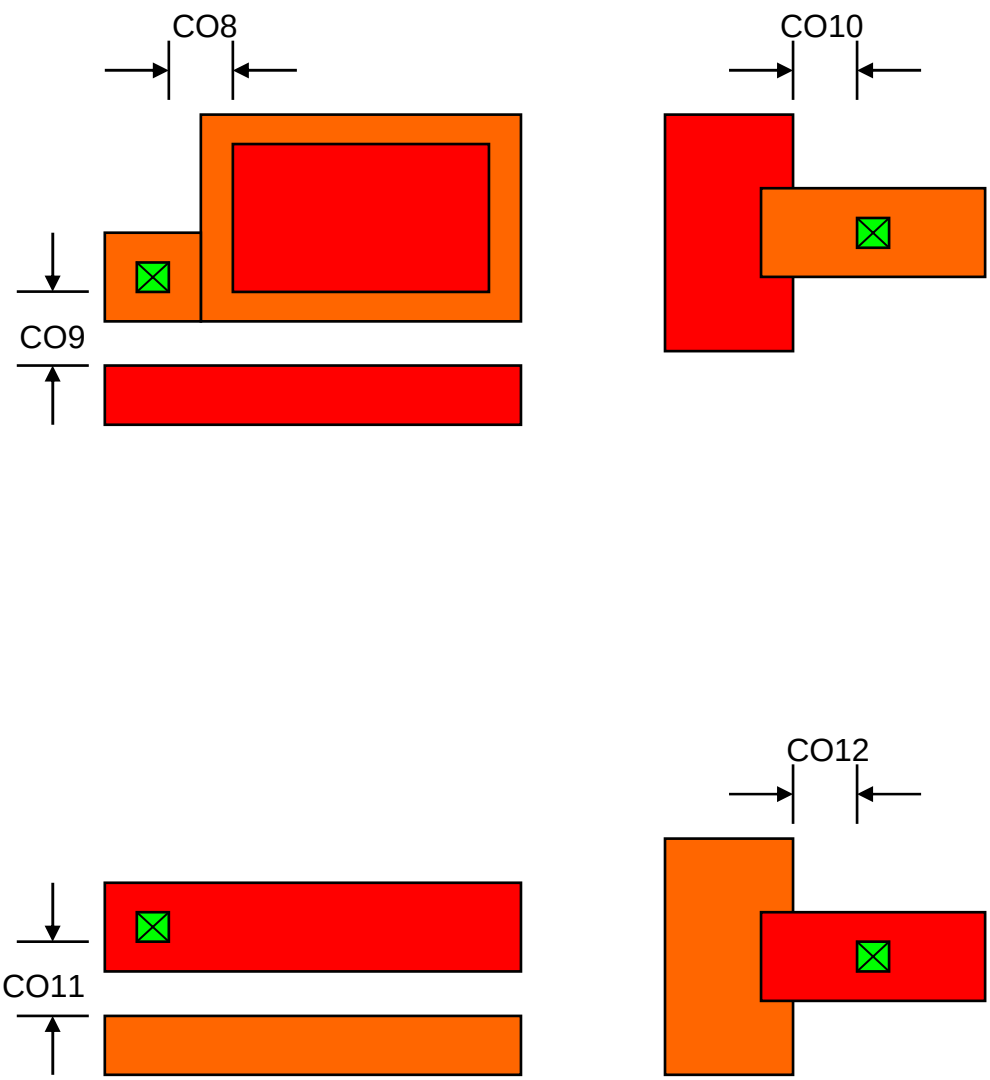
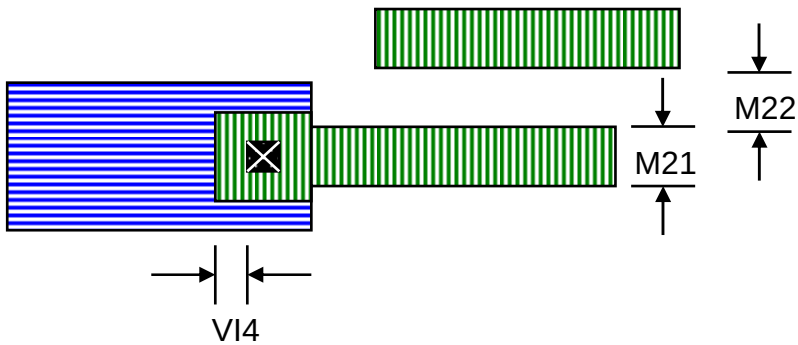
PI1
PI2
PI3



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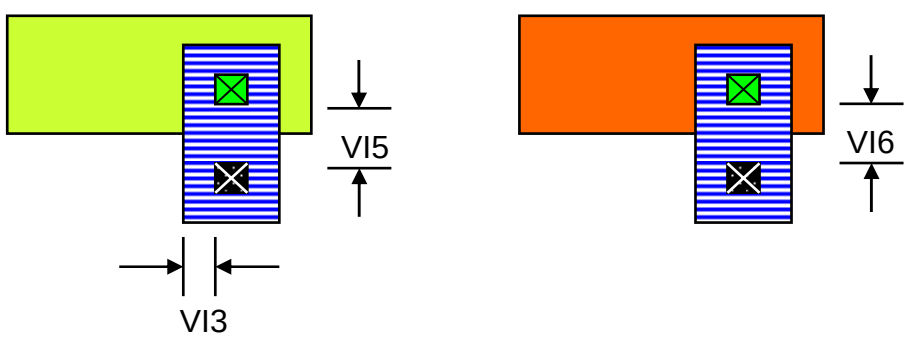
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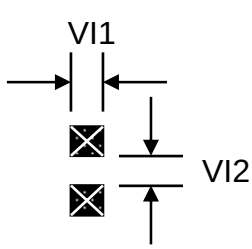
VI3


VI1
VI2

3. Process Parameters

Process Spec. (0.8μm Double Poly Metal Twin-tub CMOS)

	Thickness (Angstroms)	Capacitances	
		Area (10^{-4} pF/μm^2)	Periphery (10^{-4} pF/μm)
Gate Oxide	175±10	19.8	
Field Oxide	6300±300 (as grown)		
Poly Ⅰ	3800		
Poly Ⅱ	2000		
Poly Ⅰ/Poly Ⅱ Oxide	345	10.0	1.4
Intermediate Oxide	6000±500 (as deposited)		
Metal Ⅰ (Ti/TiN/Ti/AlSi/TiN)	300/700/500/4000/500		
Metal Ⅱ (Ti/AlSi/TiN)	500/8000/300		
Poly1 to Sub.	4700±500	0.74	0.55
Poly2 to Sub.	3500±500	0.91	0.44
Metal Ⅰ to Poly Ⅰ	5600±500	0.62	0.61
Metal Ⅰ to Sub.	9500±800	0.36	0.52
Metal Ⅰ to Diffusion	5600±500	0.62	0.63
Metal Ⅱ to Poly Ⅰ	17600±1500	0.25	0.44
Metal Ⅱ to Sub.	21500±1800	0.21	0.41
Metal Ⅱ to Diffusion	17560±1500	0.25	0.44
Metal Ⅱ to Metal Ⅰ	11500±1000	0.39	0.52
N+/P-Well Junction Depth	0.25±0.05μm	3.9	3.99
P+/N-Well Junction Depth	0.30±0.05μm	5.93	4.57

4. Electrical Parameters

(1) Sheet Resistance (I=2mA), Unit : Ω/sq.

PARMETER	MIN.	TYP.	MAX.
NWL	700	750	800
PL1	23	28	33
PL2	45	50	55
N+ Diffusion	36	40	54
P+ Diffusion	56	62	68
ME1 (Ti/TiN/Ti/AlSi/TiN)	0.05	0.06	0.07
ME2 (Ti/AlSi/TiN)	0.02	0.03	0.04

(2) Contact and Via String Resistance(Kelvin Pattern), Unit : Ω/ea.

PARMETER	MIN.	TYP.	MAX.
ME1/PL1 (0.8μm x 0.8μm)	5	10	20
ME1/PL2 (0.8μm x 0.8μm)	10	15	25
ME1/N+ (0.8μm x 0.8μm)	10	15	25
ME1/P+ (0.8μm x 0.8μm)	30	50	70
ME2/ME1 (0.8μm x 0.8μm, string)	1.0	1.5	2.5

(3) Capacitance, Unit : 10^{-4} pF/μm^2

PARMETER	MIN.	TYP.	MAX.
Gate Oxide	18.8	19.8	20.8
PL1/NWL	0.660	0.733	0.806
PL2/NWL	0.96	1.07	1.18
PL2/PL1	9.00	10.0	11.0
N+/PWL Junc., 260μm x 260μm	3.5	3.9	4.3
P+/NWL Junc., 260μm x 260μm	5.34	5.93	6.52

(4) Characteristics of Transistors

Parameter		0.8μm Technology
NMOS	2ΔL [μm]	0.03 ± 0.12
	2ΔW [μm]	0.7 ± 0.1
	Vt [V]	0.75 ± 0.1 (20/20)
		0.70 ± 0.1 (20/0.8)
	Idsat [μA/μm]	360 ± 40 (20/0.8)
	BVDSS [V]	≥ 10
PMOS	2ΔL [μm]	0.03 ± 0.17
	2ΔW [μm]	0.71 ± 0.1
	Vt [V]	-1.05 ± 0.1 (20/20)
		-1.05 ± 0.1 (20/0.8)
	Idsat [μA/μm]	-160 ± 20 (20/0.8)
	BVDSS [V]	≤ -10
Field TR	Vtn [V]	≥ 10
	BVdss [V]	≥ 10
	Vtp [V]	≤ -10
	BVdss [V]	≤ -10

5. SPICE Parameter

5.1 0.8μm Analog CMOS BSIM3 parameters (NMOSFET)

```
*
* DATE: Oct 30/01
* LOT: 01-AS027
* WAF: #05
* DIE: 1
* DEV: 0.8ASIC
* Temp= 27

.LIB CORRELATION
.PARAM
+TOXN     = 1.75E-8
+VTHON    = 0.7605623
+RSHN     = 30
+XLN      = 0
+XWN      = -1e-07
.ENDL CORRELATION

.LIB TT
.PARAM
+TOXN     = 1.75E-8
+VTHON    = 0.7605623
+RSHN     = 30
+XLN      = 0
+XWN      = -1e-07
.ENDL TT

.LIB SS
.PARAM
+TOXN     = 1.925e-08
+VTHON    = 0.8366185
+RSHN     = 33
+XLN      =  8.0e-08
+XWN      = -2e-07
.ENDL SS

.LIB FF
.PARAM
+TOXN     = 1.575e-08
+VTHON    = 0.6845061
+RSHN     = 27
+XLN      = -8.0e-08
+XWN      = 0
.ENDL FF
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```
.LIB nmos
.MODEL nmos nmos (
+VERSION = 3.2            TNOM    = 27              LEVEL   = 8
+XJ      = 2.5E-7         NCH     = 1.7E17          TOX     = TOXN
+K1      = 0.8698072      K2      = -0.0874746      VTH0    = VTHON
+K3B     = -9.740734E-3   W0      = 3.16E-6         K3      = 25.2499694
+DVT0W   = 0              DVT1W   = 0               NLX     = 4.242015E-8
+DVT0    = 1.3085931      DVT1    = 0.2493428       DVT2W   = -0.032
+U0      = 709.58018      UA      = 1.652201E-9     DVT2    = -0.1084465
+UC      = 3.942246E-11   VSAT    = 9.60767E4       UB      = 5.197043E-19
+AGS     = 0.0172207      B0      = 2.807118E-7     A0      = 0.3323353
+KETA    = -0.0114864     A1      = 0               B1      = 1E-7
+RDSW    = 1.492438E3     PRWG    = -2.830885E-4    A2      = 1
+WR      = 1              WINT    = 3.275082E-7     PRWB    = -1E-3
+XL      = XLN              XW      = XWN           LINT    = 2.148644E-8
+DWB     = 5.182712E-8    VOFF    = -0.14           DWG     = -2.284798E-8
+CDSC    = -8.730929E-4   CDSCD   = 2.978865E-5     NFACTOR = 0.8461493
+ETA0    = 0.07           ETAB    = -0.08           CDSCB   = 0
+PCLM    = 1.2750182      PDIBLC1 = 0.0128691       DSUB    = 0.5357173
+PDIBLCB = -1E-3          DROUT   = 0.1206813       PDIBLC2 = 7.22928E-4
+PSCBE2  = 1.011733E-6    PVAG    = 0.2             PSCBE1  = 2.176167E8
+RSH     = RSHN             ACM     = 2               DELTA   = 1E-3
+JS      = 3.5E-7         JSW     = 7E-13             N       = 1.013
+PRT     = 0              UTE     = -1.5            MOBMOD  = 1
+KT1L    = 0              KT2     = 0               KT1     = 0
+UB1     = -7.61E-18      UC1     = -5.6E-11        UA1     = 4.31E-9
+NQSMOD  = 0              WL      = 0               AT      = 3.3E4
+WW      = 0              WWN     = 1               WLN     = 1
+LL      = 0              LLN     = 1               WWL     = 0
+LWN     = 1              LWL     = 0               LW      = 0
+CGDO    = 3E-10          CGSO    = 3E-10           CAPMOD  = 2
+FC      = 1              CJ      = 3.9E-4          CGBO    = 1.25E-10
+MJ      = 0.41           CJSW    = 3.99E-10        PB      = 0.8
+MJSW    = 0.16           NOFF    = 1               PBSW    = 0.7
+MOIN    = 15             TPB     = 0               ACDE    = 1
+TPBSWG  = 0              TCJ     = 0               TPBSW   = 0
+TCJSWG  = 0                )                      TCJSW   = 0
*
.ENDL nmos
```

5.2 0.8µm Analog CMOS BSIM3 parameters (PMOSFET)

```
*
* DATE: Oct 30/01
* LOT: 01-AS027
* WAF: #05
* DIE: 1
* DEV: 0.8ASIC
* Temp= 27

.LIB CORRELATION
.PARAM
+TOXP     = 1.75E-8
+VTH0P    = -1.050677
+RSHP     = 60
+XLP      = 0
+XWP      = -1e-07
.ENDL CORRELATION

.LIB TT
.PARAM
+TOXP     = 1.75E-8
+VTH0P    = -1.050677
+RSHP     = 60
+XLP      = 0
+XWP      = -1e-07
.ENDL TT

.LIB SS
.PARAM
+TOXP     = 1.925e-08
+VTH0P    = -1.155745
+RSHP     = 66
+XLP      =  8.0e-08
+XWP      = -2e-07
.ENDL SS

.LIB FF
.PARAM
+TOXP     = 1.575e-08
+VTH0P    = -0.9456093
+RSHP     = 54
+XLP      = -8.0e-08
+XWP      = 0
.ENDL FF
```

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.MODEL pmos pmos (
+VERSION = 3.2          TNOM    = 27            LEVEL   = 8
+XJ      = 3E-7         NCH     = 5E16          VTH0    = VTH0P
+K1      = 0.5672916    K2      = -1.607077E-4  K3      = 6.7147332
+K3B     = -0.3632851   W0      = 2.415558E-7   NLX     = 4.017241E-8
+DVT0W   = 0            DVT1W   = 0             DVT2W   = -0.032
+DVT0    = 1.5225968    DVT1    = 0.6176352     DVT2    = -0.1796596
+U0      = 210.4145214  UA      = 1.728141E-9   UB      = 2.379788E-18
+UC      = -5.15849E-11 VSAT    = 1.275842E5    A0      = 0.7579191
+AGS     = 0.1003065    B0      = 2.807118E-7   B1      = 1E-7
+KETA    = -3.6043E-3   A1      = 0             A2      = 0.909
+RDSW    = 2.988385E3   PRWG    = -2.912297E-5  PRWB    = -1E-3
+WR      = 1            WINT    = 2.845986E-7   LINT    = 3.593413E-8
+XL      = XLP            XW      = XWP         DWG     = -2.802105E-8
+DWB     = 4.34232E-8   VOFF    = -0.1404518    NFACTOR = 1.3793807
+CDSC    = -5.187898E-4 CDSCD   = 2.978865E-5   CDSCB   = 0
+ETA0    = 0.1096558    ETAB    = -0.04         DSUB    = 0.6483395
+PCLM    = 4.5366292    PDIBLC1 = 0.3492589     PDIBLC2 = 9E-4
+PDIBLCB = 0            DROUT   = 0.5492665     PSCBE1  = 9.374553E9
+PSCBE2  = 1E-8         PVAG    = 5.3654134     DELTA   = 0.0125296
+RSH     = RSHP           ACM     = 2             N       = 1.013
+JS      = 2.5E-7       JSW     = 3.5E-13       MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = 0
+KT1L    = 0            KT2     = 0             UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+NQSMOD  = 0            WL      = 0             WLN     = 1
+WW      = 0            WWN     = 1             WWL     = 0
+LL      = 0            LLN     = 1             LW      = 0
+LWN     = 1            LWL     = 0             CAPMOD  = 2
+CGDO    = 3E-10        CGSO    = 3E-10         CGBO    = 1.12E-10
+FC      = 1            CJ      = 5.93E-4       PB      = 0.8
+MJ      = 0.47         CJSW    = 4.57E-10      PBSW    = 0.7
+MJSW    = 0.26         NOFF    = 1             ACDE    = 1
+MOIN    = 15           TPB     = 0             TPBSW   = 0
+TPBSWG  = 0            TCJ     = 0             TCJSW   = 0
+TCJSWG  = 0             )
*
.ENDL pmos
```

6. Appendices

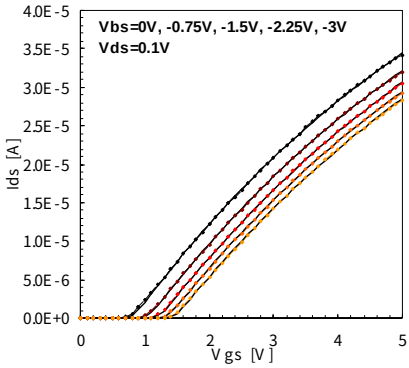
A-1. nMOS Experiment vs. Simulation

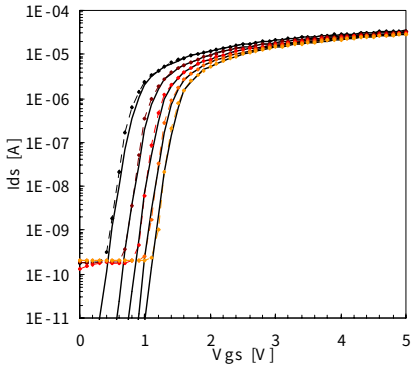
A-2. pMOS Experiment vs. Simulation

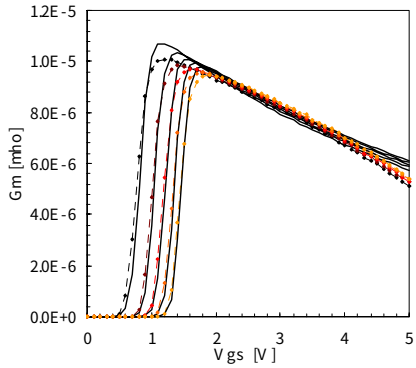
A-1. nMOS Experiment vs. Simulation_W/L=20/20, unit=μm

Symbol : Experimental Data
Solid Line : Model Results

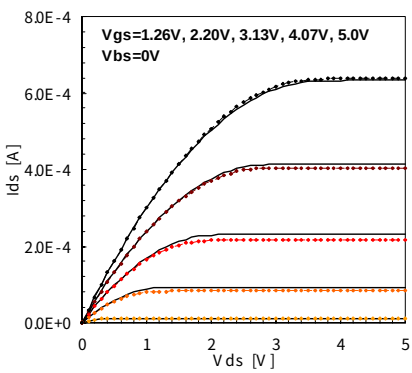
(a). ID/VG-VB (VD=0.1V)

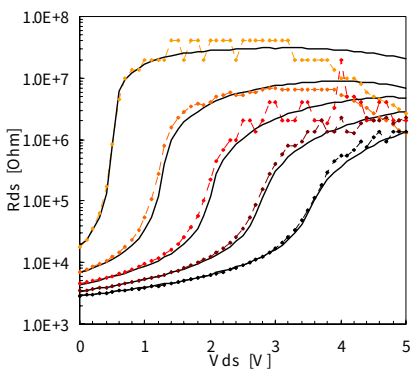


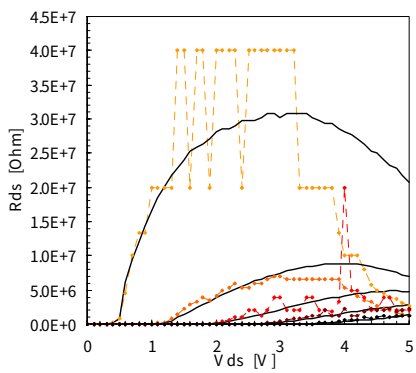




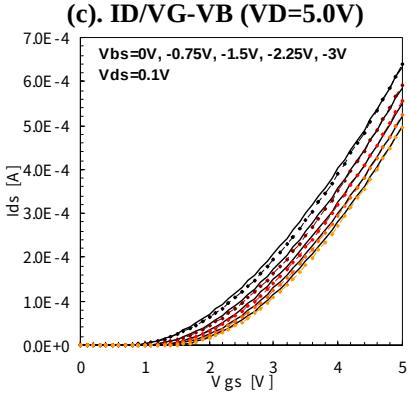
(b). ID/VD-VG (VB=0V)

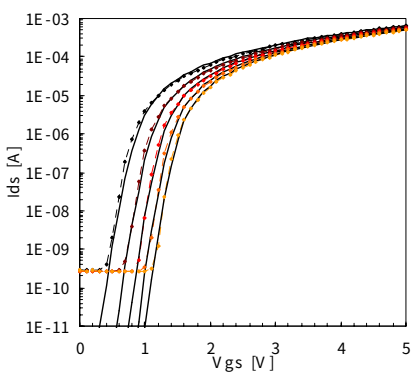


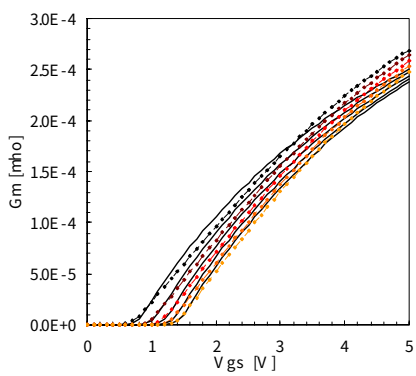




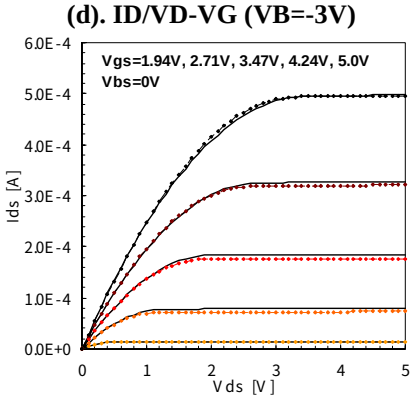
(c). ID/VG-VB (VD=5.0V)

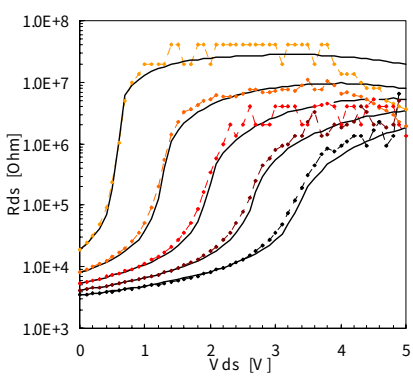


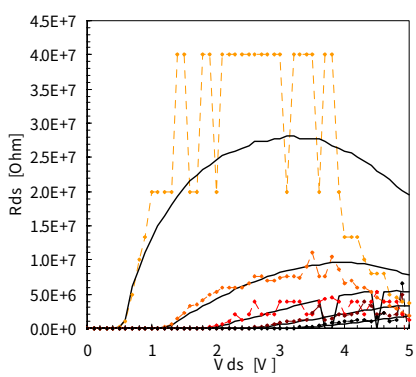




(d). ID/VD-VG (VB=-3V)



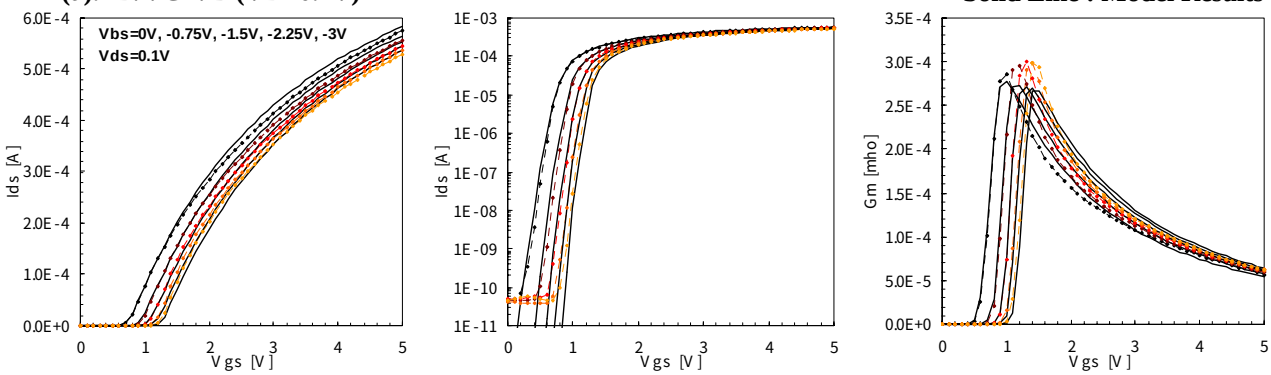




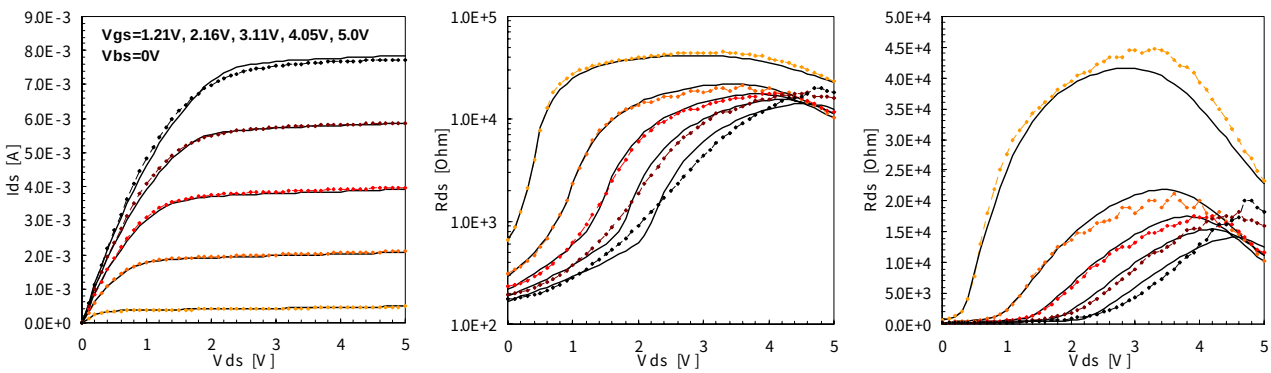
A-1. nMOS Experiment vs. Simulation(계속)_W/L=20/0.7, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

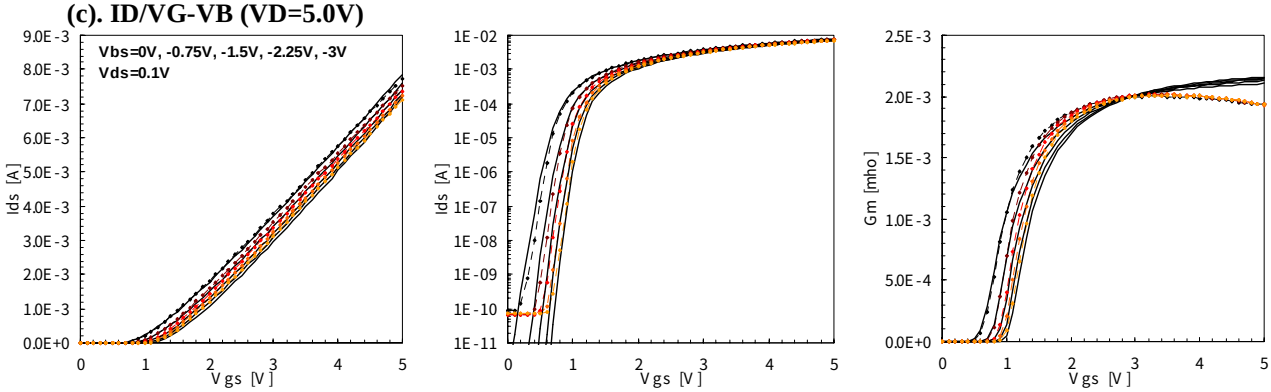
(a). ID/VG-VB (VD=0.1V)



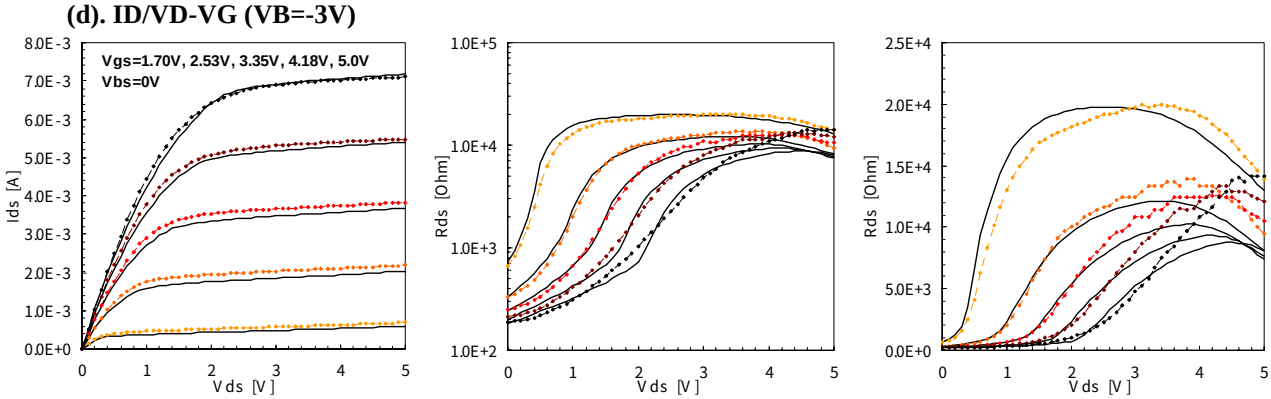
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=5.0V)



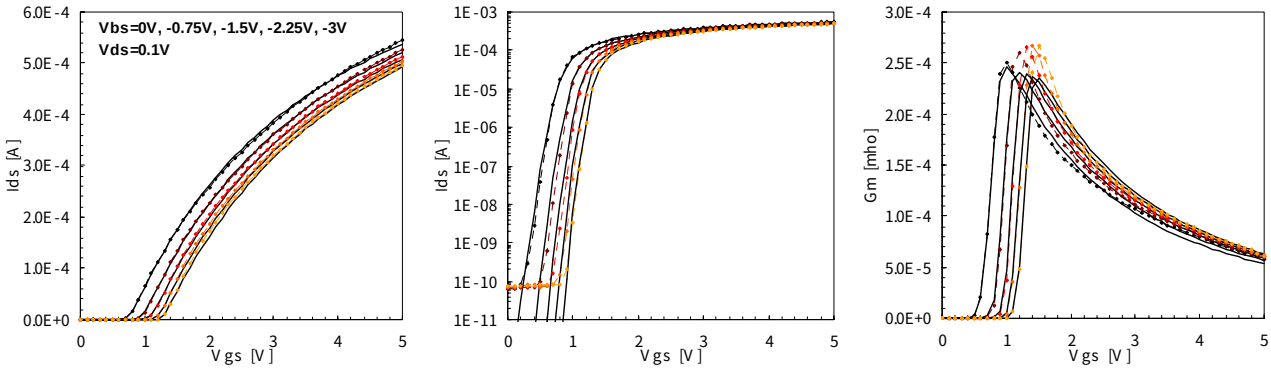
(d). ID/VD-VG (VB=-3V)



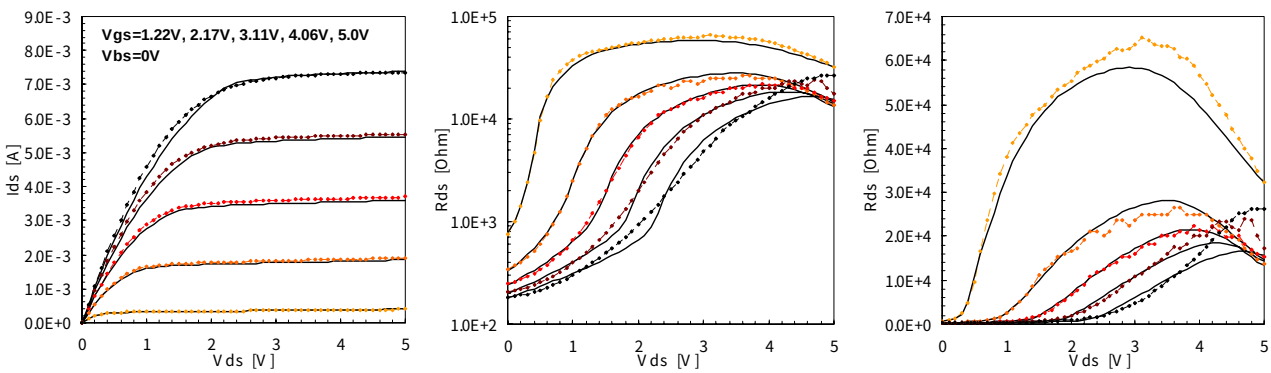
A-1. nMOS Experiment vs. Simulation(계속)_W/L=20/0.8, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

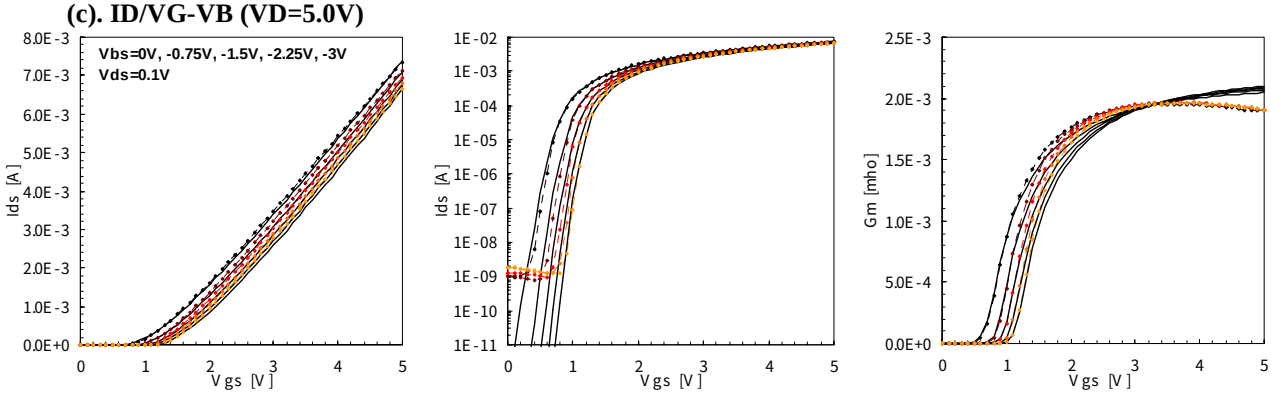
(a). ID/VG-VB (VD=0.1V)



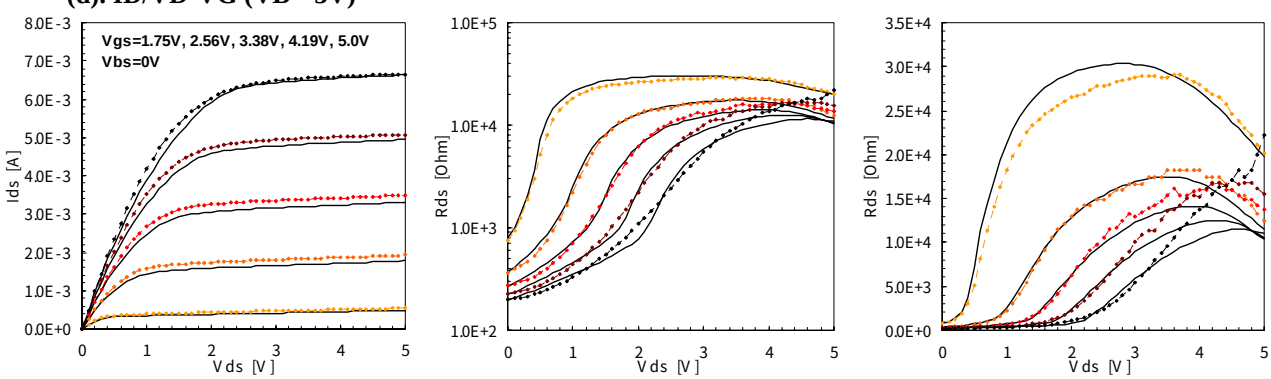
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=5.0V)



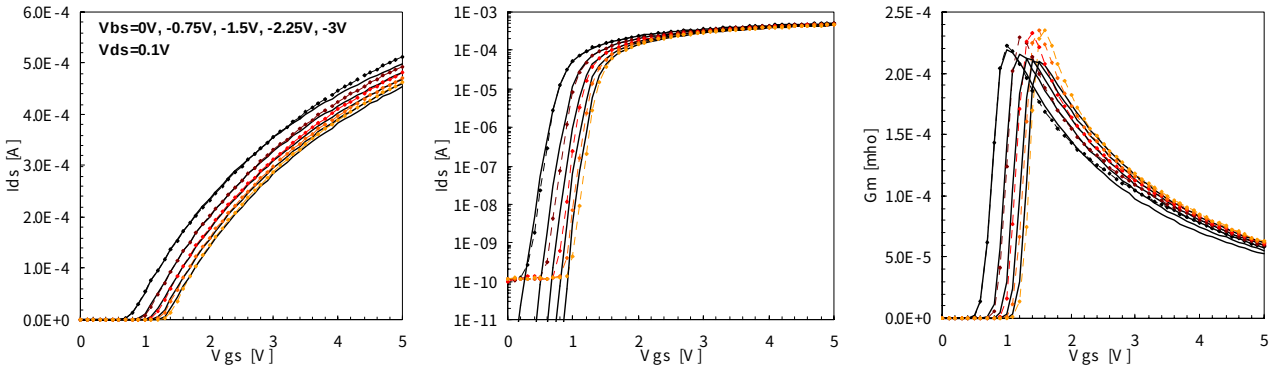
(d). ID/VD-VG (VB=-3V)



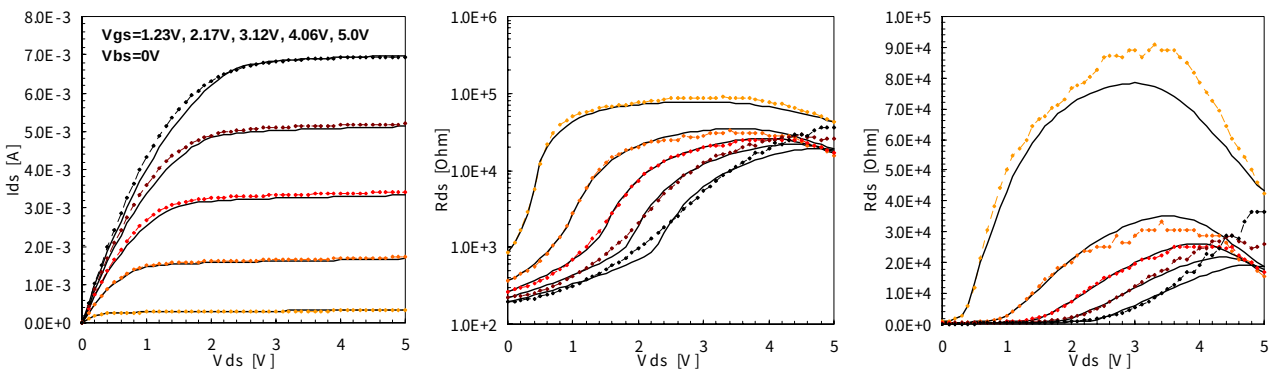
A-1. nMOS Experiment vs. Simulation(계속)_W/L=20/0.9, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

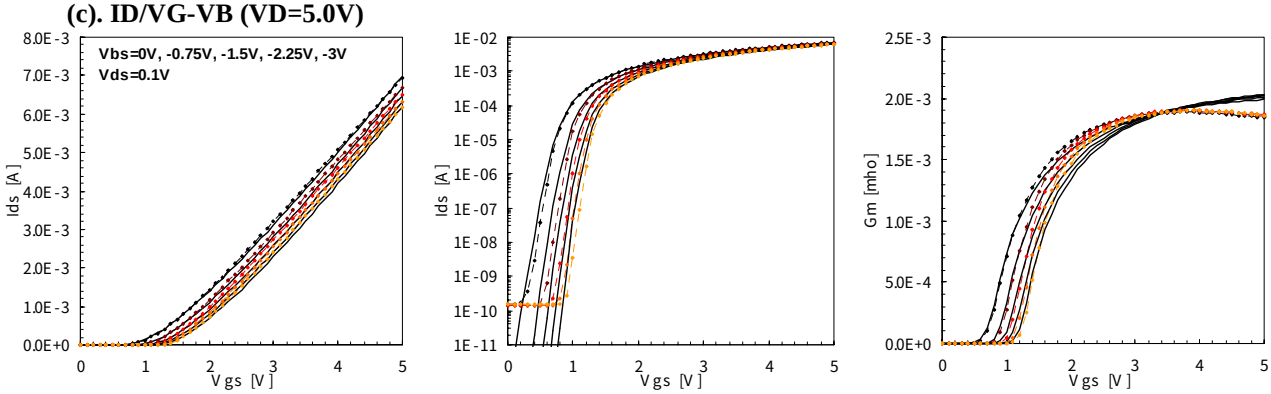
(a). ID/VG-VB (VD=0.1V)



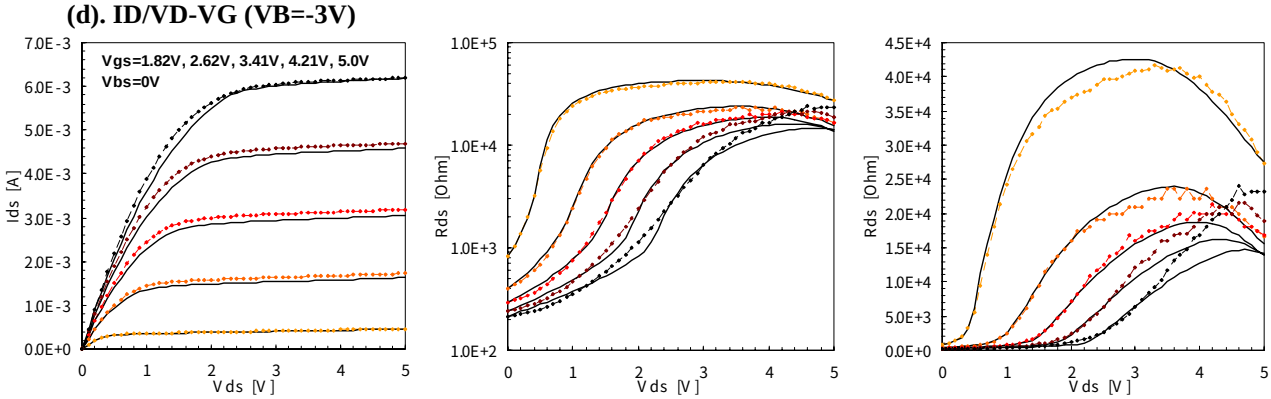
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=5.0V)



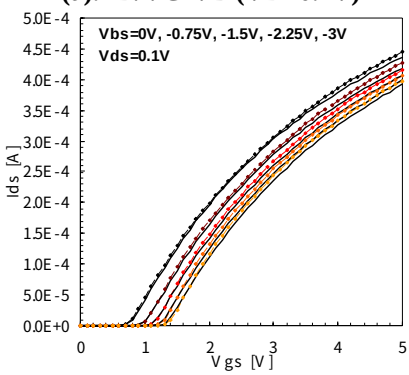
(d). ID/VD-VG (VB=-3V)

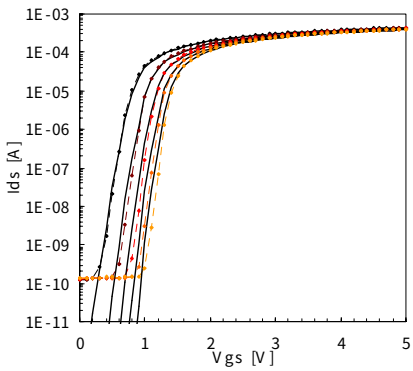


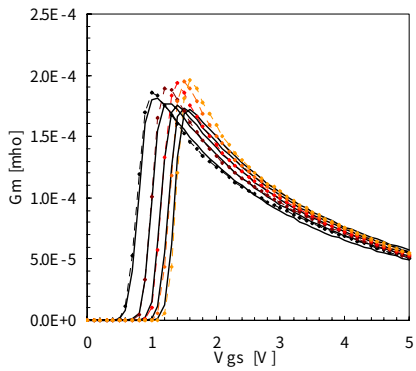
A-1. nMOS Experiment vs. Simulation(계속)_W/L=20/1.1, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

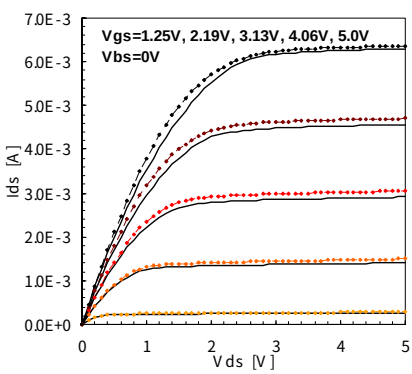
(a). ID/VG-VB (VD=0.1V)

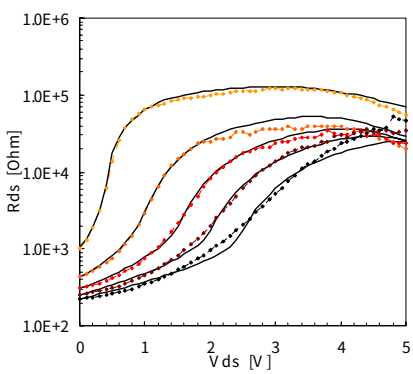


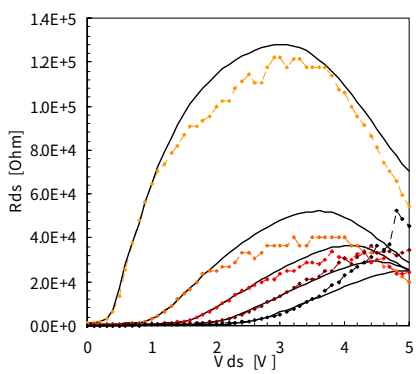




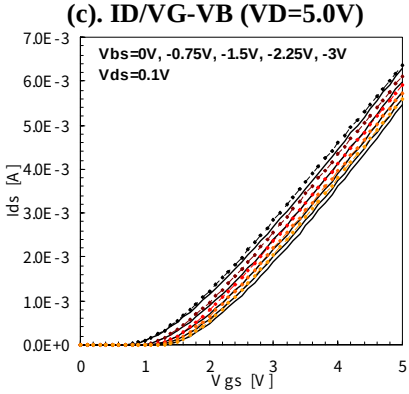
(b). ID/VD-VG (VB=0V)

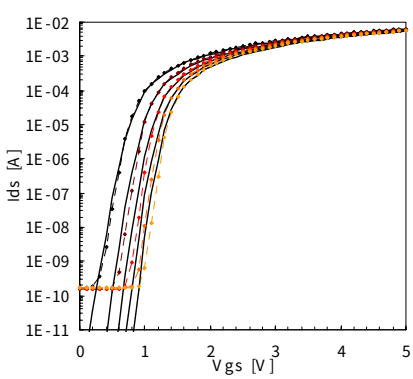


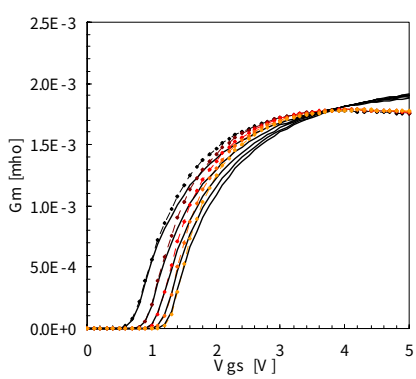




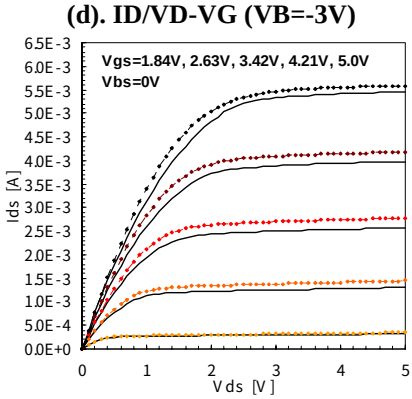
(c). ID/VG-VB (VD=5.0V)

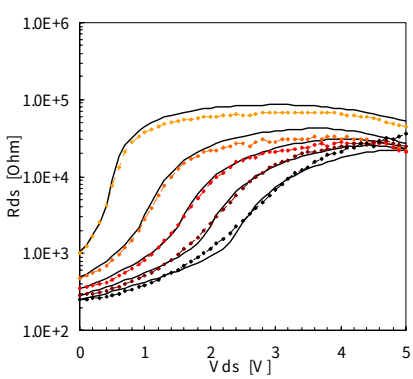


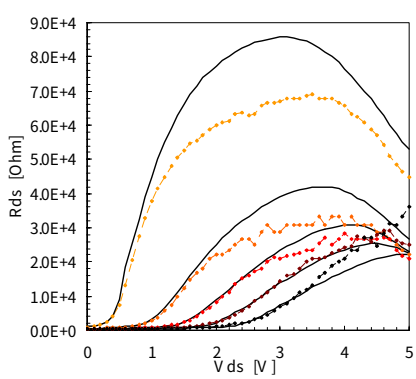




(d). ID/VD-VG (VB=-3V)



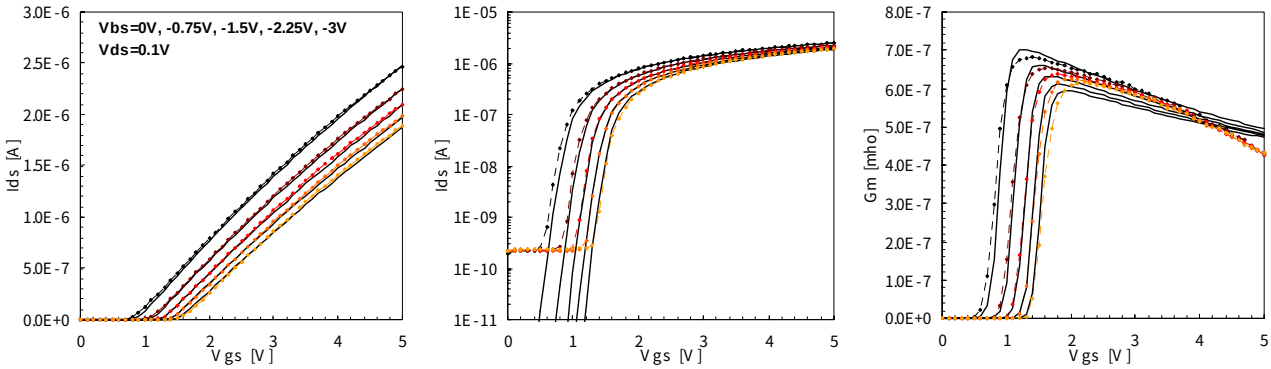




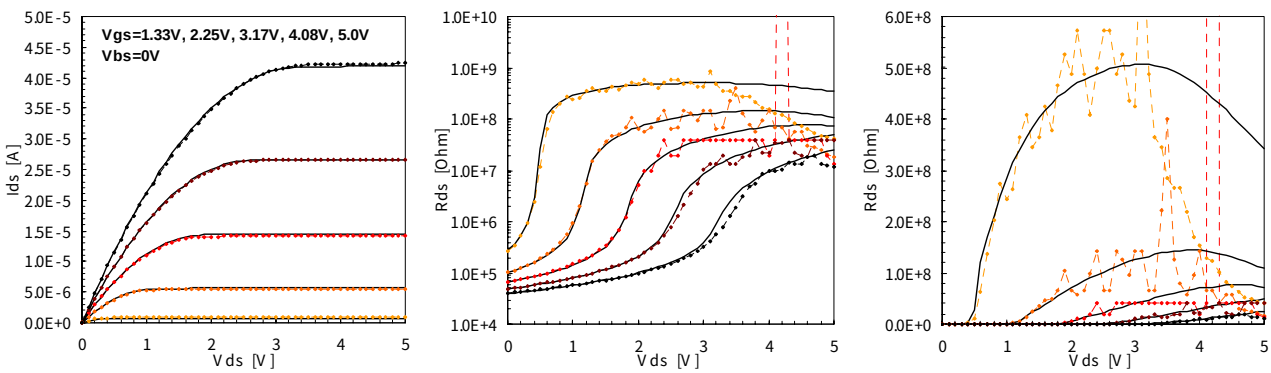
A-1. nMOS Experiment vs. Simulation(계속)_W/L=2/20, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

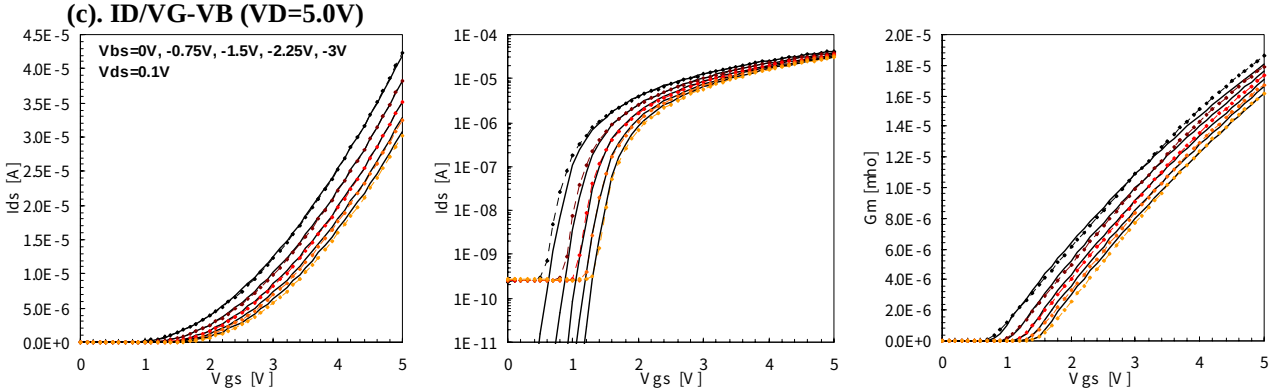
(a). ID/VG-VB (VD=0.1V)



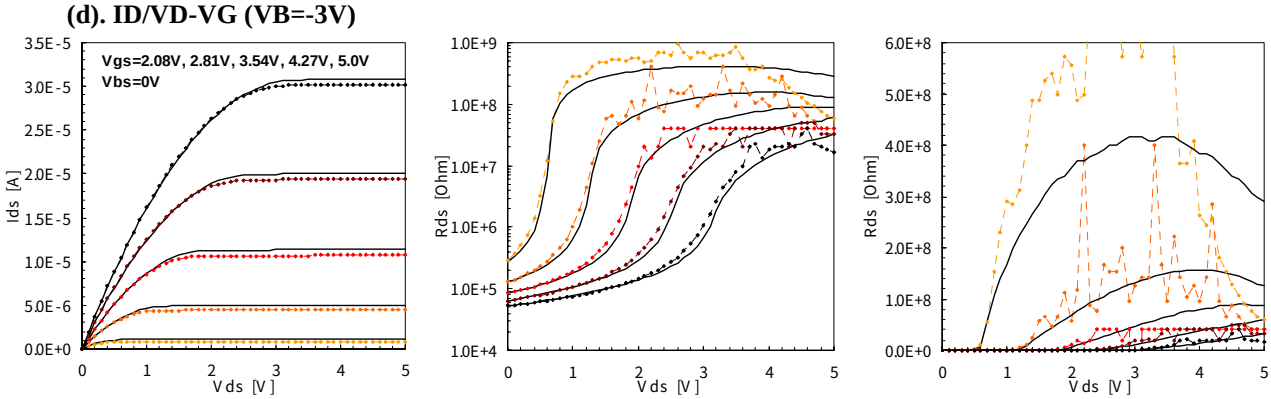
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=5.0V)



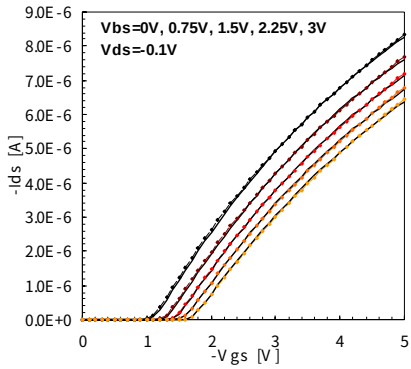
(d). ID/VD-VG (VB=-3V)

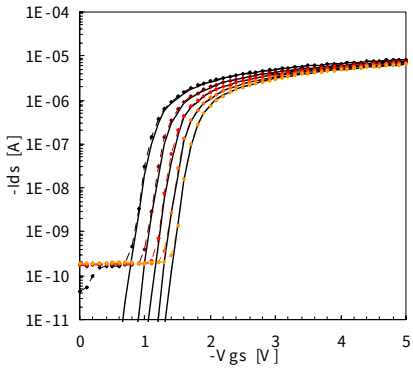


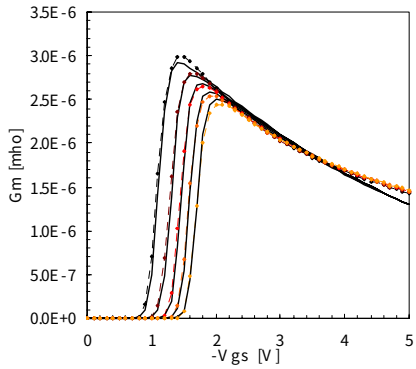
A-2. pMOS Experiment vs. Simulation_W/L=20/20, unit=μm

Symbol : Experimental Data
Solid Line : Model Results

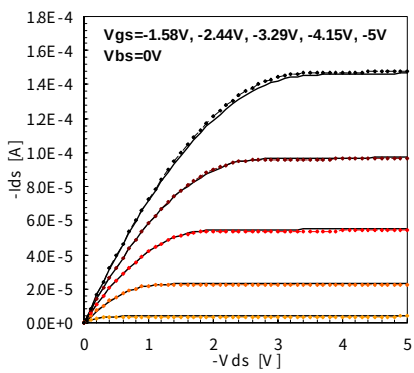
(a). ID/VG-VB (VD=-0.1V)

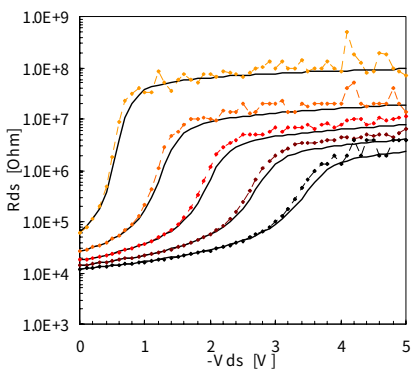


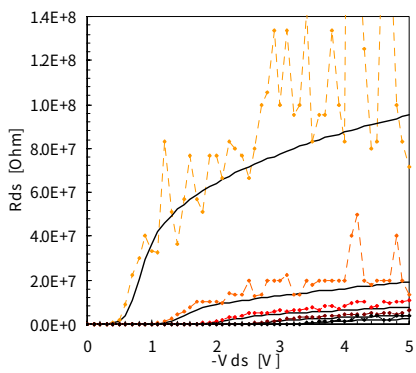




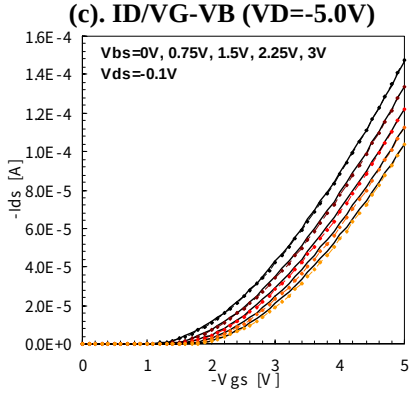
(b). ID/VD-VG (VB=0V)

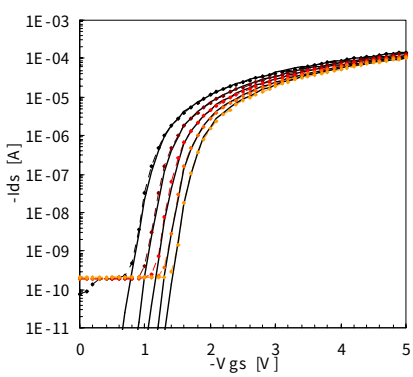


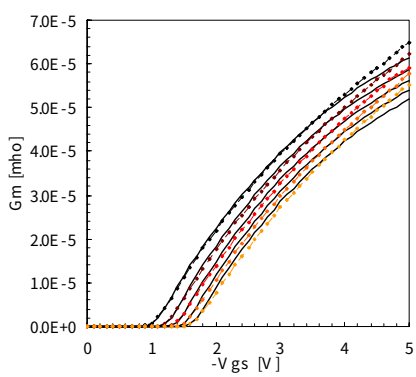




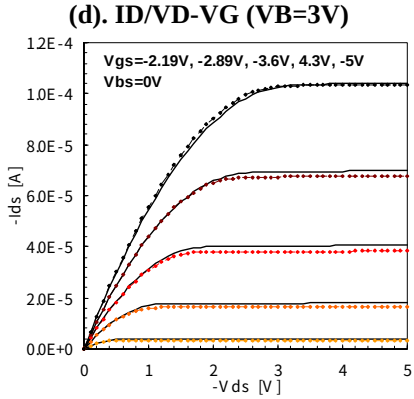
(c). ID/VG-VB (VD=-5.0V)

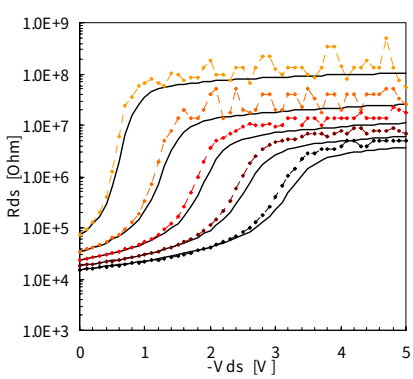


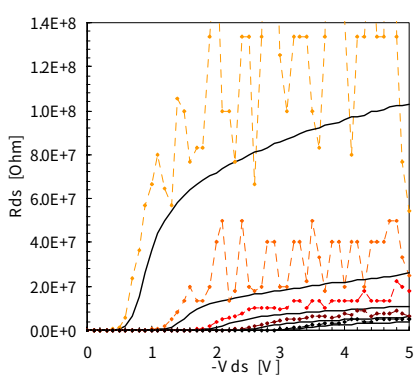




(d). ID/VD-VG (VB=3V)



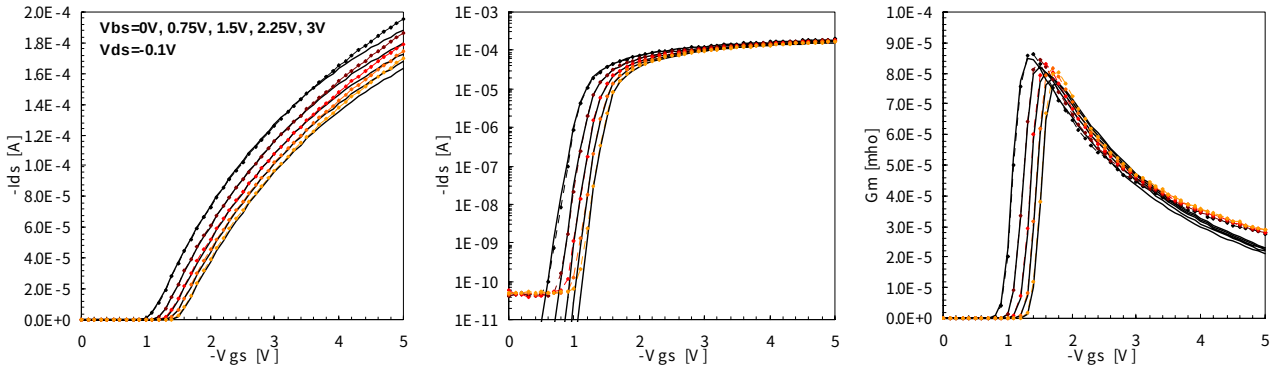




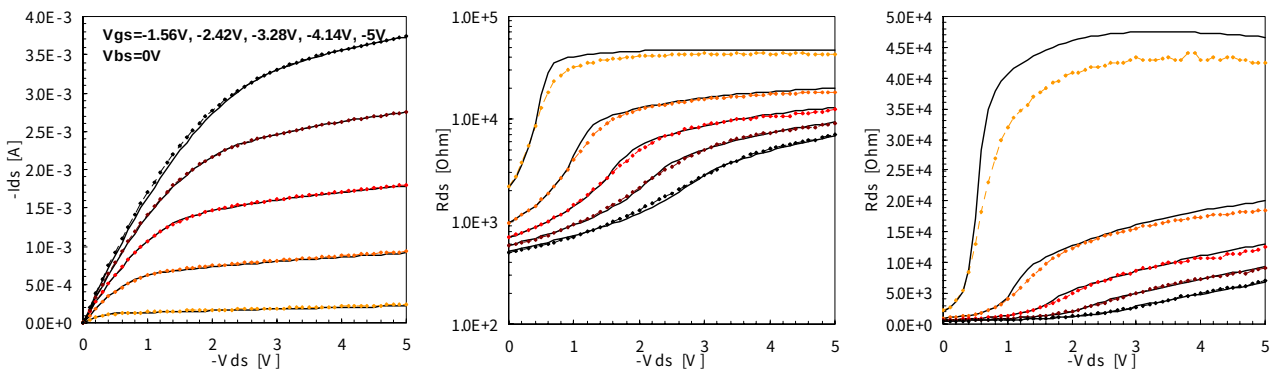
A-2. pMOS Experiment vs. Simulation(계속)_W/L=20/0.7, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

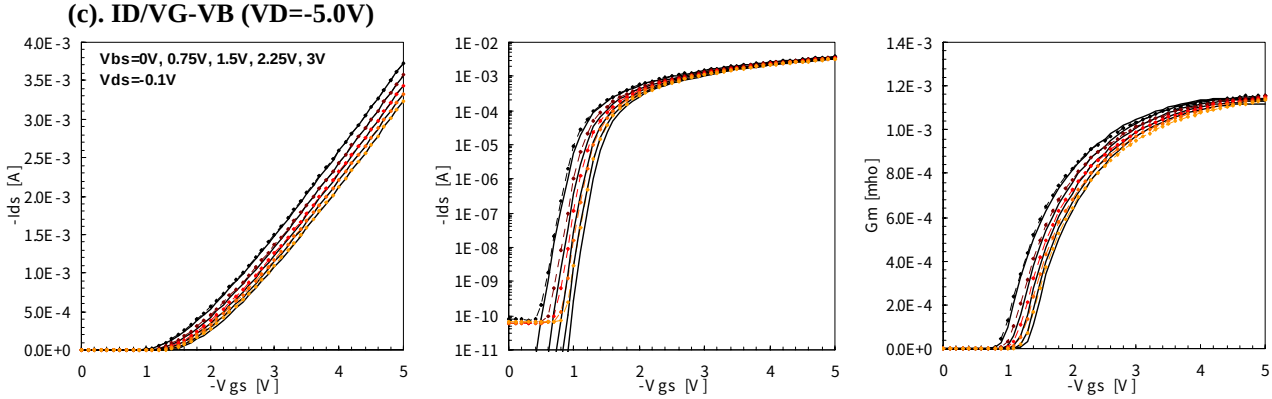
(a). ID/VG-VB (VD=-0.1V)



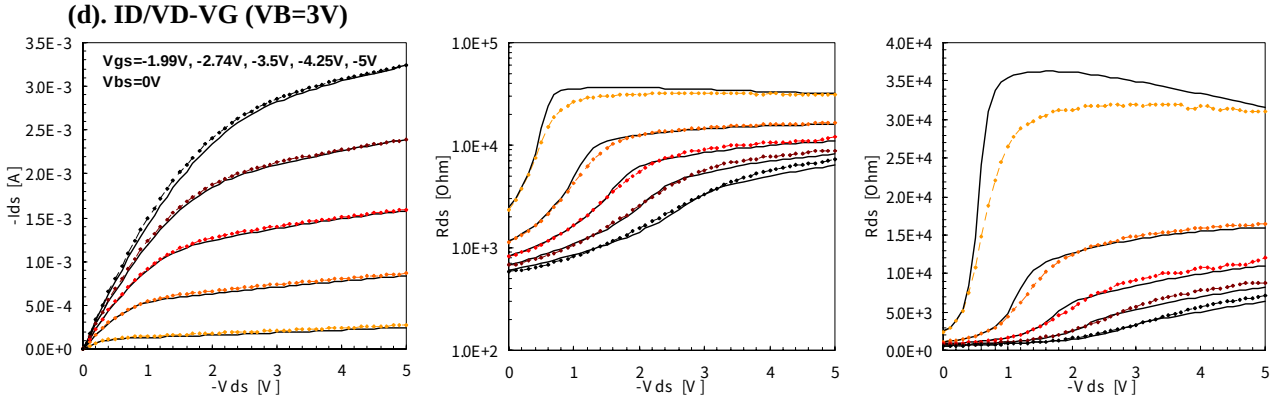
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=-5.0V)



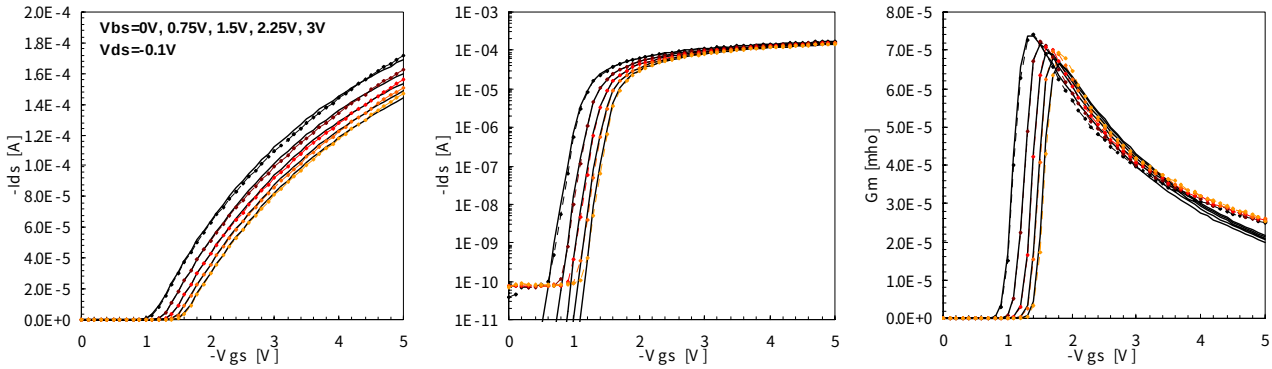
(d). ID/VD-VG (VB=3V)



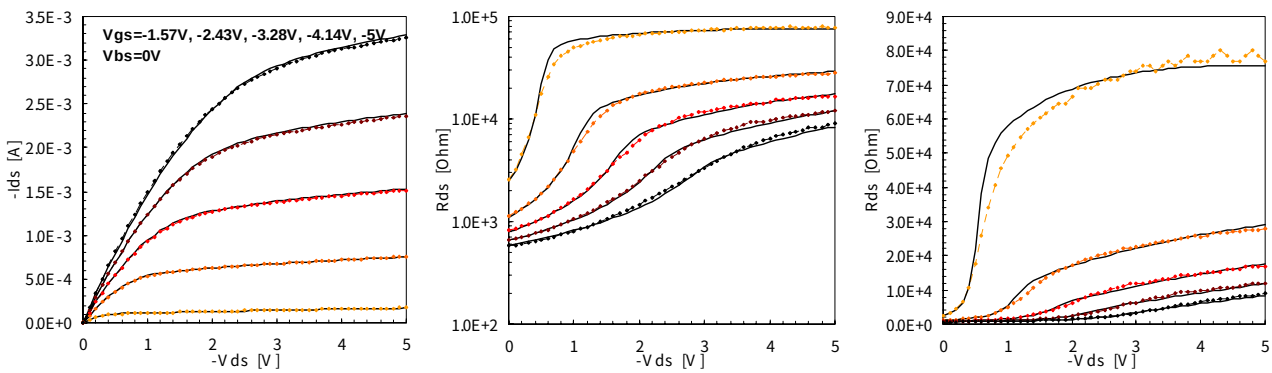
A-2. pMOS Experiment vs. Simulation(계속)_W/L=20/0.8, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

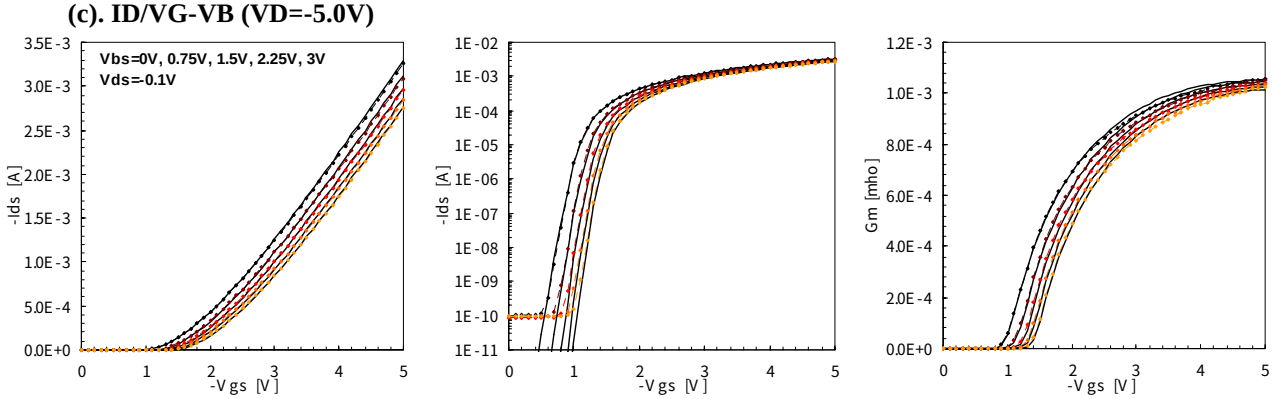
(a). ID/VG-VB (VD=-0.1V)



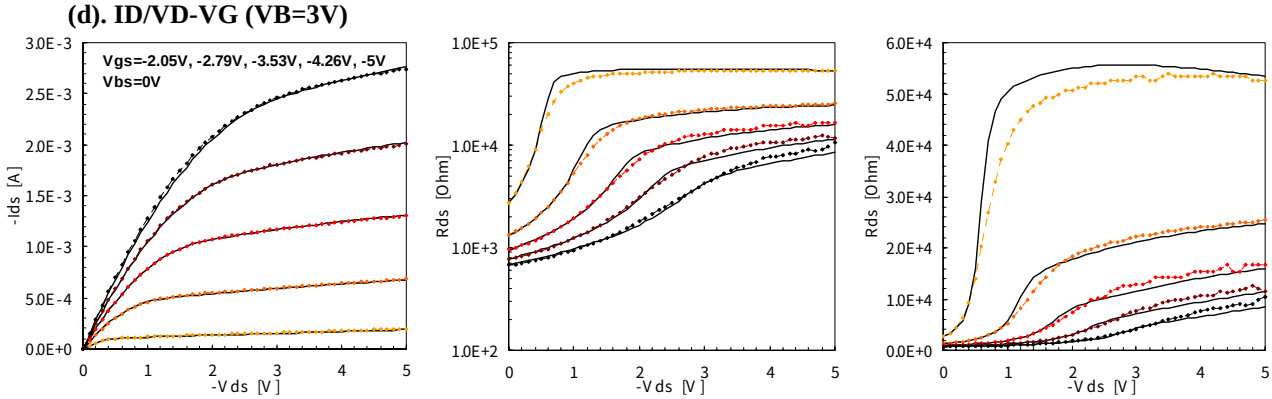
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=-5.0V)



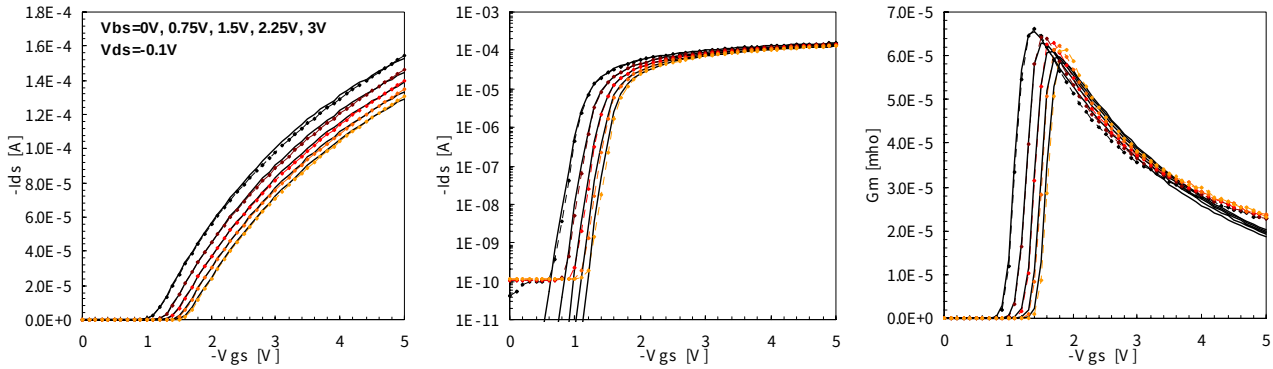
(d). ID/VD-VG (VB=3V)



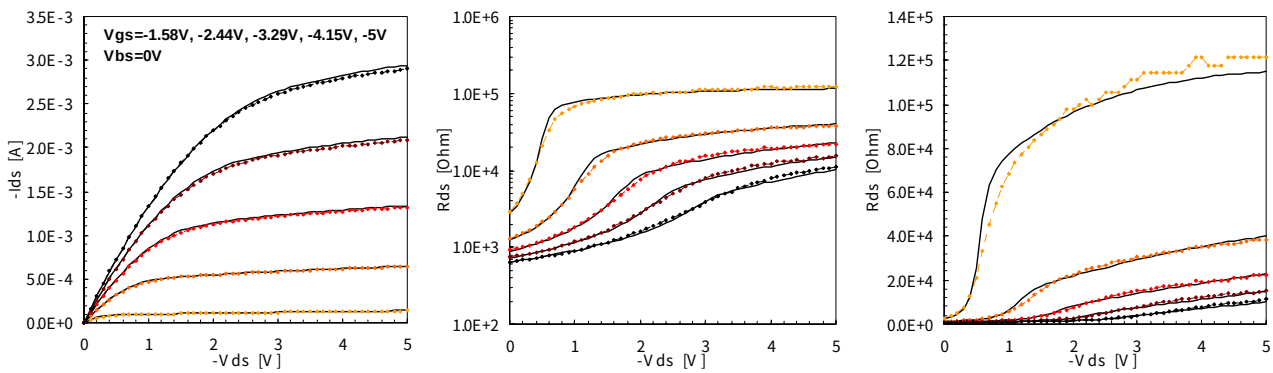
A-2. pMOS Experiment vs. Simulation(계속)_W/L=20/0.9, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

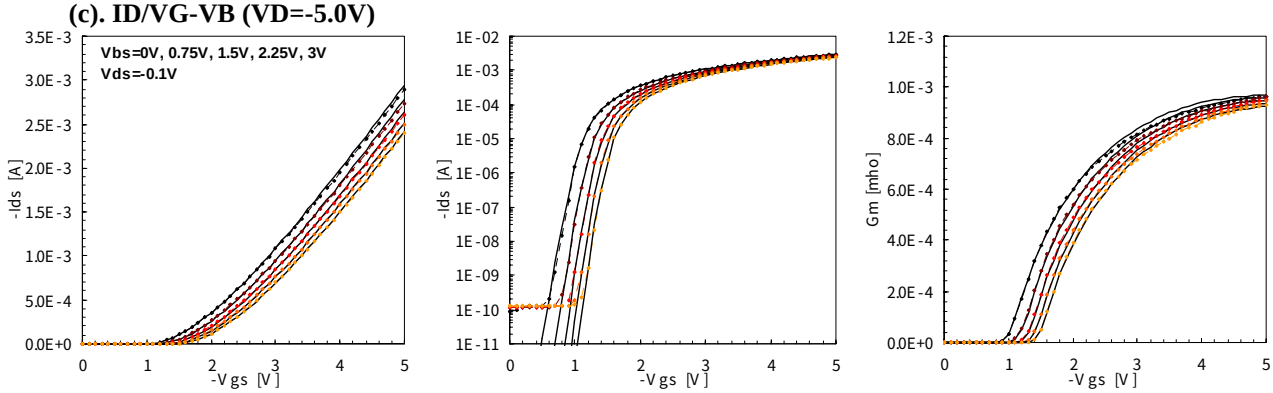
(a). ID/VG-VB (VD=-0.1V)



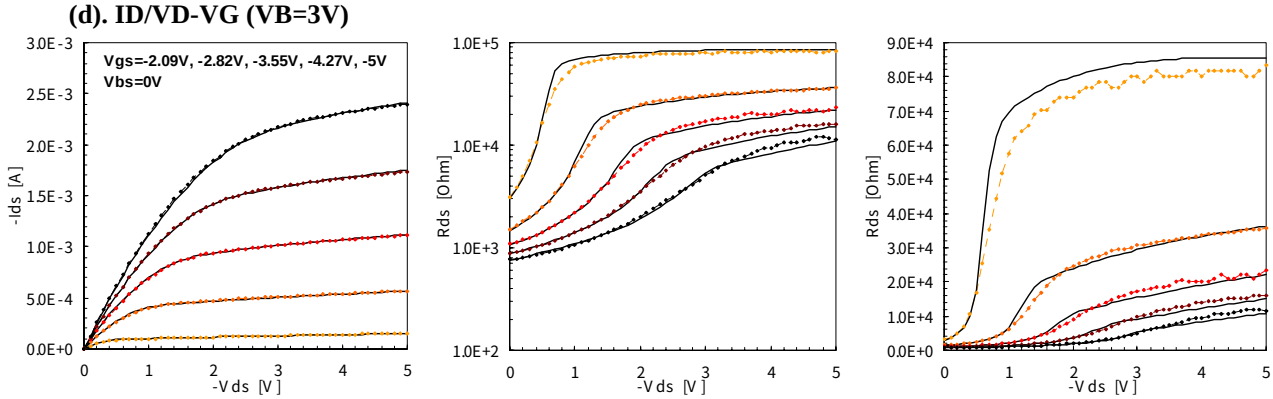
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=-5.0V)



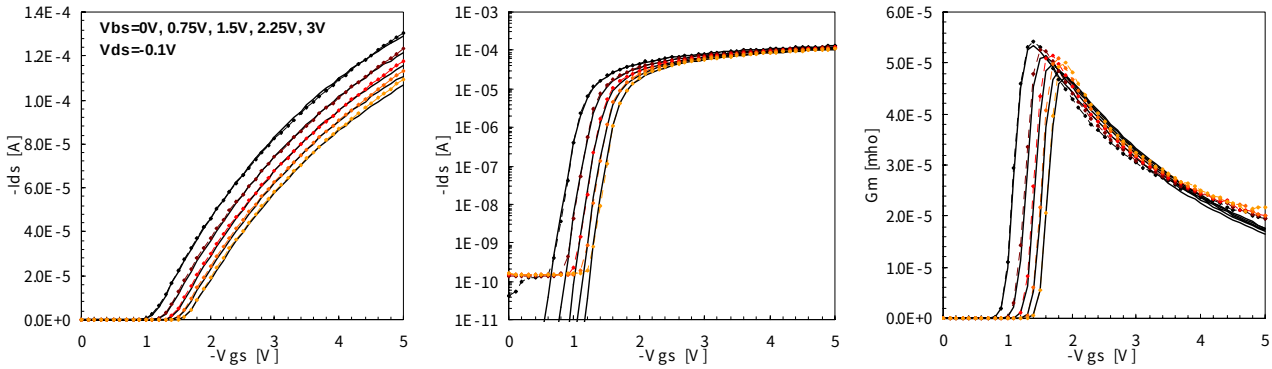
(d). ID/VD-VG (VB=3V)



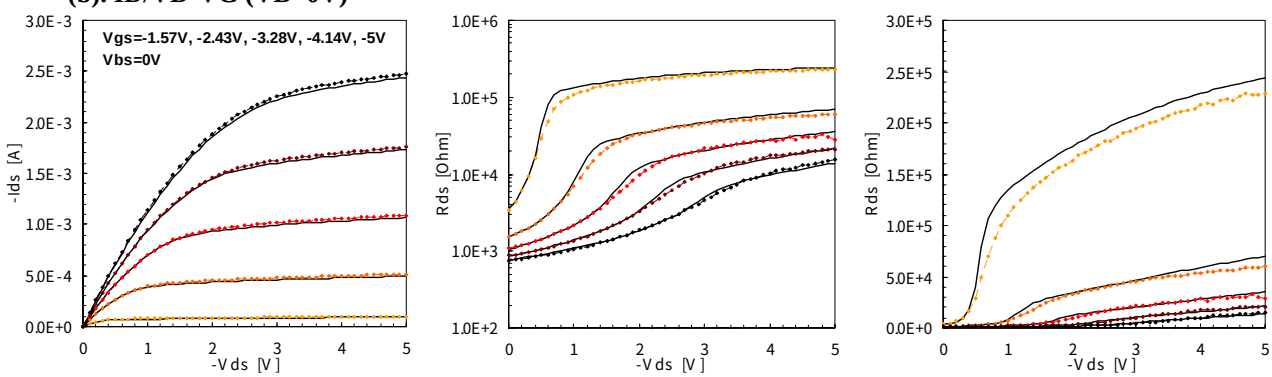
A-2. pMOS Experiment vs. Simulation(계속)_W/L=20/1.1, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

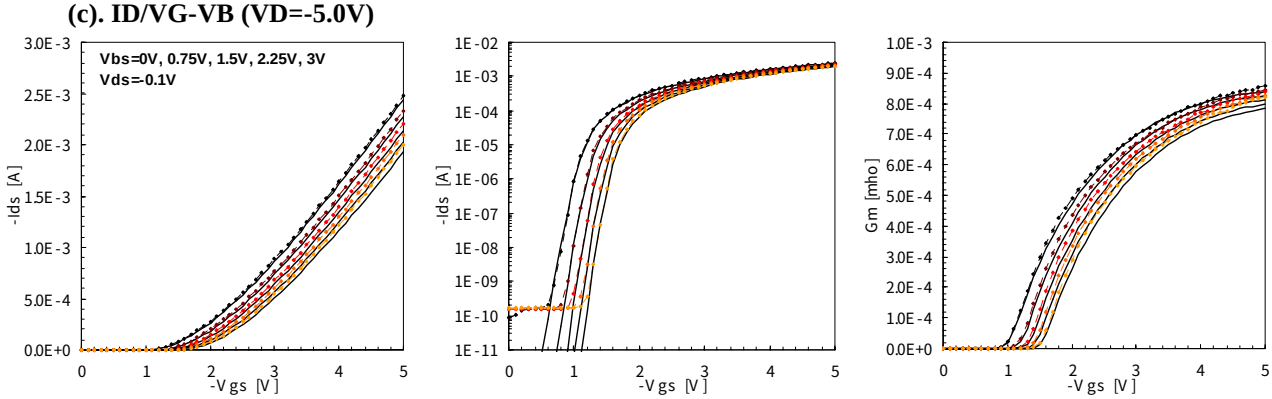
(a). ID/VG-VB (VD=-0.1V)



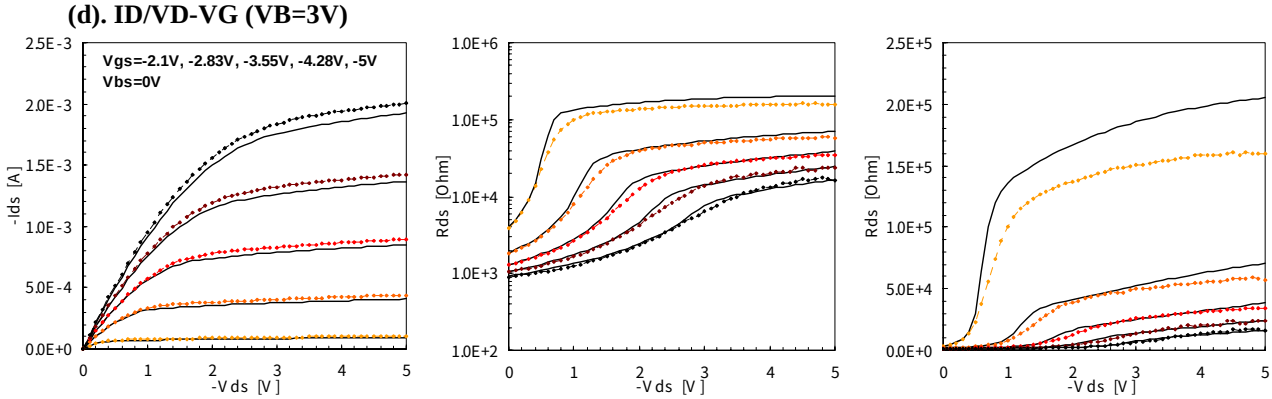
(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=-5.0V)



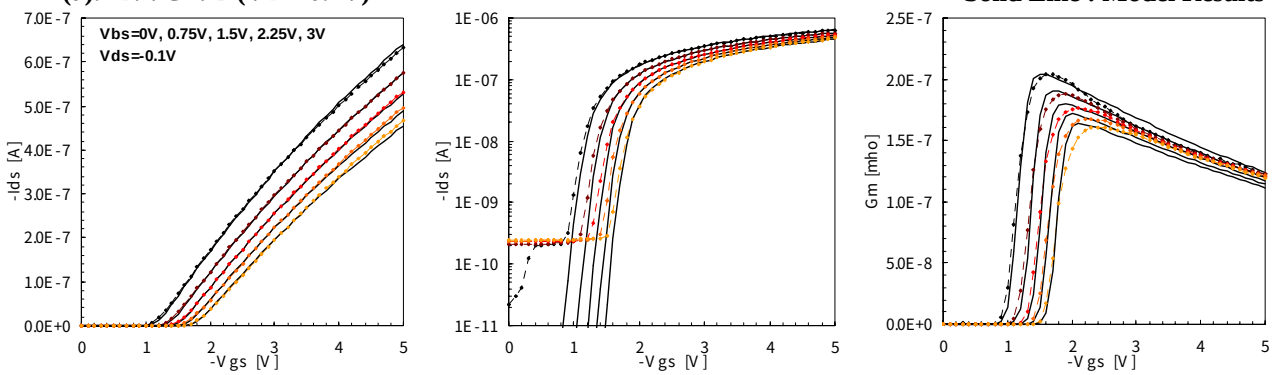
(d). ID/VD-VG (VB=3V)



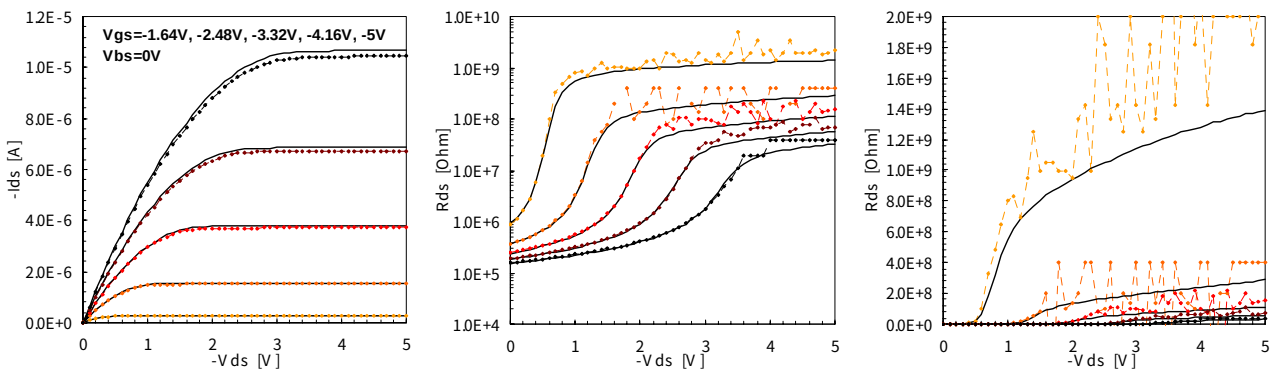
A-2. pMOS Experiment vs. Simulation(계속)_W/L=2/20, unit=㎛

Symbol : Experimental Data
Solid Line : Model Results

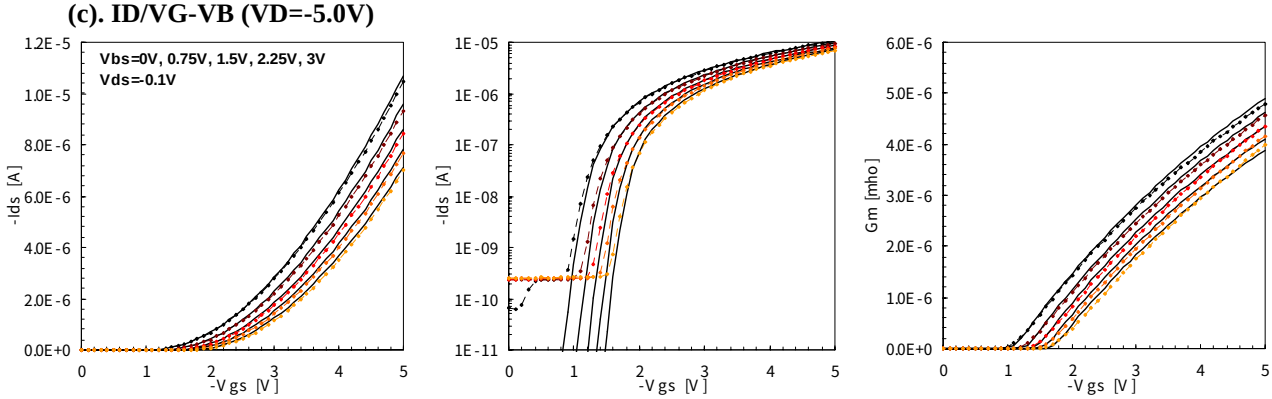
(a). ID/VG-VB (VD=-0.1V)



(b). ID/VD-VG (VB=0V)



(c). ID/VG-VB (VD=-5.0V)



(d). ID/VD-VG (VB=3V)