For mobile robot and micro industrial instruments

Aldebaran Microcontroller SoC for Mobile Robot (Low Power MCU Core Technology)

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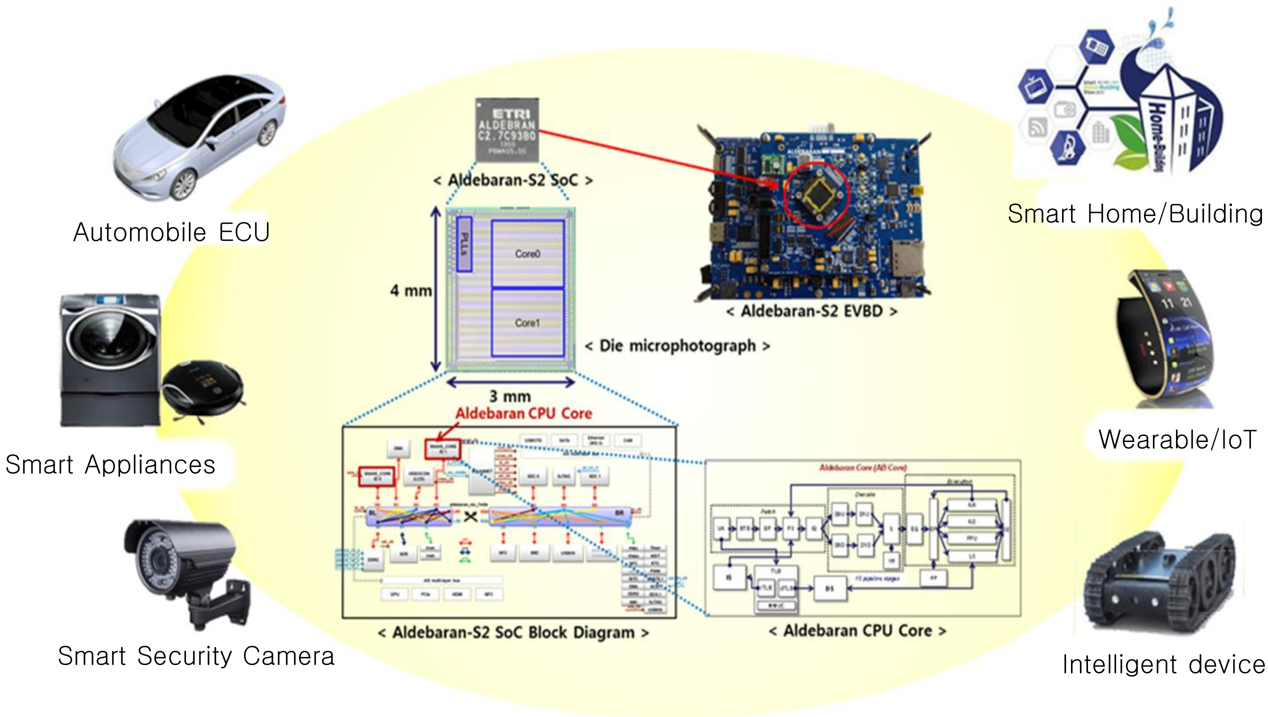
TECHNOLOGY BRIEF

Low Power MCU Core Technology

▣ Technology Overview

- High performance processor technology specialized for mobile computing applications
- Low power multi-core processor technology based on dynamic energy regulation architecture
- Fault-tolerant architecture for automotive application and unmanned vehicle
- Real-time parallel processing support including video encoding/decoding and DSP



☐ Keywords

Application Processor, Fault Tolerance, Mobile Robot, Low-power, Interface Integration

☐ TRL

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Technology Classification Code		
Sector	Sub Sector	Industry
Intelligent Semiconductor	Intelligent Semiconductor	Intelligent Semiconductor

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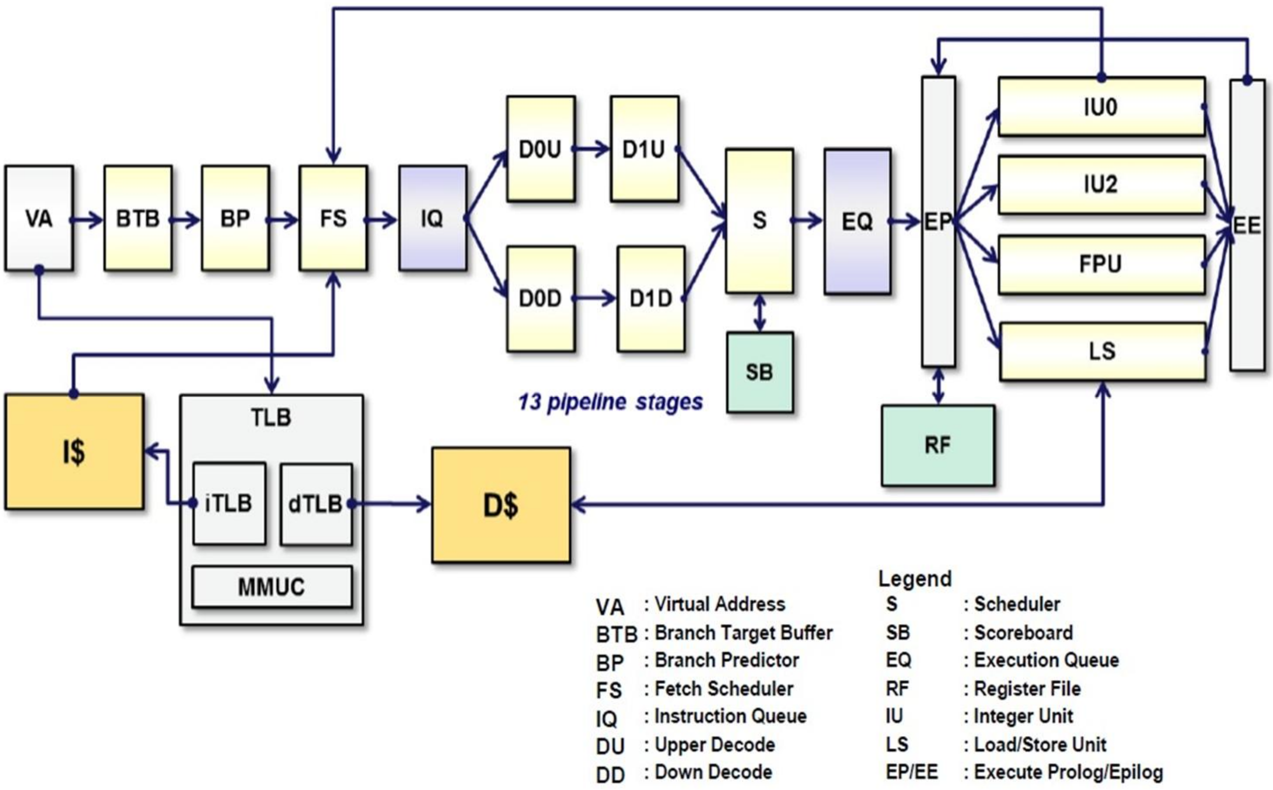
TECHNOLOGY BRIEF

Low Power MCU Core Technology

▣ Technology Description



[Low-power MCU Core Architecture]

▶ Specifications of low-power MCU Core

- Dual-issue in-order superscalar 32bit MCU
- Low-power MCU Core
- BTB: 2-way x 256-entry x 58-bit = 3.7Kbytes
- BP: 10-bit GHR, 256 x 16 x 2b = 1Kbyte
- I/D cache: Each 32K bytes, Tag 2.12Kbytes, 1$ + D$ 68.25Kbytes
- Dual-rail decode and in-order scheduler with Scoreboard

☐ Target Application

▶ **Automotive ECU, unmanned mobile vehicle, drone, wearable device**

▣ Outstanding Features

Aldebaran, the low-power microcontroller SoC based on superscalar architecture is developed by ETRI's own technology. The proposed SoC integrates legacy I/F, fault-tolerant safety micro-architecture, and DSP processor technology for automotive and unmanned robot applications.

▶ Key Features and target application field

- Fault-tolerant architecture: Malfunction of automotive ECU directly threaten drivers' safety. Considering the road vehicle's functional safety standard, ISO 26262, Aldebaran SoC is composed with exquisitely designed fault-tolerant multi-core and cache architecture which operate as dual-core lockstep and support ECC checksum. The dual-core lockstep architecture compares each core's processing result every cycle and ECC checksum detects a bit flip on cache data. These fault-tolerant and recovery schemes guarantee the functional safety of Aldebaran SoC.

- Various peripherals and applications: Aldebaran SoC provides various serial interfaces for actuator and sensor control. It includes multiple channels of JTAG, CAN 2.0 A/B FD, UART, GIOCAP, PWM, I2C, SPI, QEI. Image and video processing modules are also included such as video input/output module and decoder/encoder. In addition RTOS is ported to support real time applications.

- Low-power design: For mobile wearable and unmanned vehicle applications, design methodology for low power consumption is applied to Aldebaran SoC and its cores. Aldebaran SoC consumes 0.24mW/MHz, one of the best power efficiency ever achieved in SoC industry.

- Aldebaran SoC and all peripherals mentioned above are ETRI's own property. All design technology and relative rights are protected by patents.

▣ IPR Status

Korean patent : 4 articles applied

▣ Technology Trend

Rapid growth of electric devices in automobile component attracts IT companies to focus on the automotive field as the next mobile platform. In addition, recently emerging mobile robot technology requires real-time high performance and interface integrated application processor.

▶ Massive demands on high performance and robust MCU

- Automotive applications: Emerging safety issues on vehicle induce the establishment of ISO 26262: 'Road vehicles – Functional safety'. After the period of the operation frequency and performance competition, the upcoming core technology on automotive ECU is the fault detection and recovery technique. All MCU vendors are concentrating on designing robust ECU micro-architecture and applying for patents about fault-tolerance schemes.

- Autonomous vehicle applications: IT and automotive companies slowly move the controllability of the automobile from human to automotive ECUs, ultimately aiming autonomous vehicle. The way on fully autonomous vehicle, driving assist systems are evolving such as ABS, LDWS/LKAS, FCW. These system requires high performance and real-time OS ported automotive processor.

☐ Korea

- Most of Korean system-semiconductor companies have imported foreign processor IP paying expensive loyalties because of the absence of domestic high-performance embedded processor and software technology.

- In case of small businesses, expensive cost of processor IP reduces the opportunity of the innovative product with a competitive price.

- Major companies are spending enormous expenses to IP licensing. The effort for developing their own processor core is inefficient and insufficient.

☐ Global

- ARM Co. provides various solutions differentiated by performance and power consumption through Cortex™ product line based on ARMv7 architecture.

- Apple, Samsung, Nvidia, Qualcomm develops AP by integrating their own IP based on ARM Co.'s. Thus, dominance of ARM Co. in mobile processor market is being intensified.

▣ Market Trend

Explosive growth of mobile multiprocessor is expected. On 2018, more than 10 billion mobile device market (10 times of PC) is expected.

***Reference : Morgan Stanley**

▶ Domestic and foreign mobile processor market scale (unit: Foreign - $1 million, Domestic - 100 million ₩)

Classification		Year of 1st (2015)	Year of 2nd (2016)	Year of 3rd (2017)	Year of 4th (2018)	Year of 5th (2019)
Mobile SoC	Foreign	160	167	200	233	300
	Domestic	1000	2000	2333	2500	2667

▶ Domestic and foreign mobile processor market share (unit: %)

Classification		Year of 1st (2015)	Year of 2nd (2016)	Year of 3rd (2017)	Year of 4th (2018)	Year of 5th (2019)
Mobile SoC	Foreign	0	3	10	15	20
	Domestic	5	10	15	20	40

☐ Market Leaders

▶ Current World Leading Vendors

- Apple, Nvidia, Qualcomm

▶ Current Domestic Leading Vendors

- Samsung etc.

☐ Technology Demand

Application	Microcontroller SoC for unmanned mobiles include cognitive robot, autonomous automobile
Industry	Microcontroller SoC of mobile robots for industrial machinery, distribution, farming, forestry

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▣ Scope of Technology Transfer

- **The proposed technology is "Low-power MCU Core Technology", which run and compile algorithm written in C/Assembly for various digital signal processing with MCU core. Entire technology is listed below.**

- Dual-issue in-order superscalar 32bit MCU
- Low-power MCU core
  - High-performance mode: 0.24mW/MHz@800MHz,65nm
  - Low-power mode: 0.08mW/MHz@300MHz,0.7V
- BTB: 2-way x 256-entry x 58-bit = 3.7Kbytes
- BP: 10-bit GHR, 256 x 16 x 2b = 1Kbyte
- I/D cache: Each 32K bytes, Tag 2.12Kbytes, I$ + D$ 68.25Kbytes
- Dual-rail decode and in-order scheduler with Scoreboard
- Execution queue
  - Queue containing decoded/scheduled blocks
  - Run-time OS support for LP execution
- Superscalar execution unit
  - 2 integer units, 1 load store, and FPU for single/double floating point operations
  - Multi-port register file

▣ Applications and Effects

▶ Applications

- The main application of proposed technology is the automotive processor supporting fault detect and recovery schemes.

- Unmanned vehicle, drone, mobile application processor and video/image processing are also supported with various peripherals.

▶ Effects

- Low-power MCU core is a key component of system-semiconductor and the MCU design technology is directly related to the technological competitiveness of domestic system-semiconductor industry.

- Securement and propagation of ETRI's own MCU processor to domestic system-semiconductor industry with reasonable prices will strengthen the price competitiveness of domestic system-semiconductor industry.